DATASHEET SHORT – epc670

3D TOF imager 320 × 240 pixels

General description

The epc670 is a fully integrated 3D-cwTOF imager with a resolution of 320 × 240 pixels (QVGA). As a system on chip, the epc670 contains next to the CCD pixel field the complete control logic to operate the device. The output of the chip is 12 bit DCS distance data per pixel, which are accessible through a mobile industry processor interface (MIPI).

Only a few additional components are needed to build a complete 3D camera. A distance resolution in the millimeter range for distances up to 20 meters while ensuring eye safety standards is feasible. Up to 700 full frame TOF images per second are delivered in rolling mode. The extremely high sensitivity of the chip allows low illumination power and reduced overall power consumption compared to other TOF imagers.

Key Features

- Exceptional QE in NIR: 72% @ 905 nm
- High ambient light immunity for outdoor applications
- Ultra-high frame rate: up to 700 TOF fps (54 Mpixel/s)
- High sensitivity of 8 e-/LSB
- High TOF dynamic range: 32 dB for a single integration time
- Simultaneous grayscale image, day and night
- Mobile industry processor interface (MIPI, CSI-2 over D-PHY)
- Internal or external modulation clock for multi-camera setups
- SIL2 ready

Block diagram

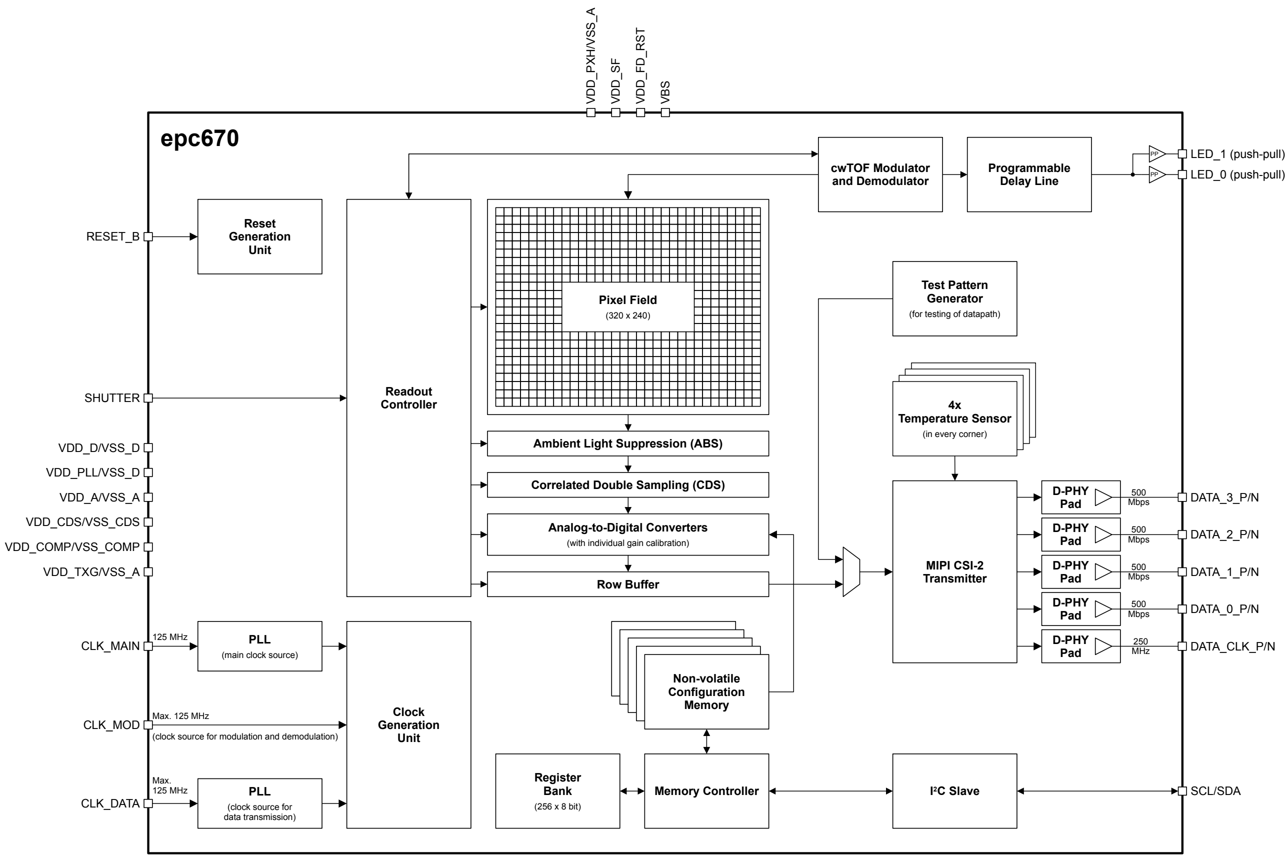


Figure 1: High-level functional block diagram

Main features

- **General**
  - Full monolithic design
  - 320 × 240 pixel field
  - Global shutter
  - Up to 54 million 3D data points per second
  - Back-illuminated, 100% fill factor pixel design
  - Active illumination range: visible to IR up to 1000 nm
    - Anti-reflective coating optimized for 900 to 940 nm
  - Automatic suppression of ambient light on pixel level in the charge domain
  - Full daylight operation
  - Selectable gain in the range of 0.25 to 4
  - 4 integrated temperature sensors
- **Optical data**
  - Pixel pitch of 20 µm × 20 µm
  - Sensitivity of 8 electrons per LSB (@ gain of 4)
  - 12 bit ADC resolution
  - TOF dynamic range of >32 dB (one integration time)
- **Mobile industry processor interface (MIPI)**
  - D-PHY v1.2 physical layer
    - 4 differential data lanes (500 Mbps per lane, 2 Gbps in total)
    - 1 differential clock lane (250 MHz)
  - CSI-2 v2.1 protocol layer
- **I^2C control interface**
- **Integrated non-volatile memory**
  - Calibration
  - User-programmable parameters
  - Unique chip ID
- **Frame configuration table**
  - Pre-configuration of up to 16 DCS frames per burst triggered by a single shutter (e.g., integration time, modulation frequency, region of interest, etc.)
- **Flexible clocking**
  - Separate input clocks for main part of the sensor, modulation and data transmission
  - Up to 125 MHz input clock each
- **Functional safety features**
  - Predefined test patterns
    - Full scale (stripes)
    - Ramp (gradient)
    - PN9 (pseudo-random)
  - Metadata including temperature data per MIPI frame
  - CRC protection of transmitted data on MIPI CSI-2 protocol level
  - Selectable ADC output test values which can be used to check ADC counters, data handling and data transmission
  - Parity checking for processed readout sequencer code
  - Register and sequencer RAM dump over MIPI
- **Packaging**
  - Back-illuminated flip-chip SMD mounting
  - Cost optimized 79 pin CSP, 11.7 mm × 9.3 mm
  - RoHS compliant
- **Other data**
  - -40 °C to +125 °C operating range

Measurement modes

- **Modulation**
  - Sinusoidal modulation
  - Selectable modulation frequencies from 0.625 MHz to 31.25 MHz resulting in unambiguity distances of 4.8 m to 240 m
  - 2 illumination control pins which can be controlled individually
- **Distance measurement modes**
  - 700 fps with 4 DCS rolling mode (full pixel field)
  - 350 fps with 2 DCS (full pixel field)
  - 175 fps with 4 DCS (full pixel field)
  - Ultra-fast measurement by reduction of the image field (ROI)
  - Shutter release input for precise start/stop and single/continuous measurement control
- **Non-distance light measurement modes**
  - Ambient light measurement (grayscale image without active illumination)
  - Grayscale image with active illumination
- **Resolution reduction**
  - Readout of only every second row and/or column
  - Increased frame rate for reduced number of rows
- **Region of interest (ROI)**
  - Rectangular sub-pixel-field readout
  - Increased frame rate or reduced power consumption

1. Typical application setup

A typical system-level setup is shown in Figure 2. After ramping up the supplies, enabling the clock sources and releasing the reset, the epc670 can be configured over I^2C, e.g. to set the integration time. ToF DCS image bursts can then be obtained by pulsing the shutter pin. Alternatively, DCS bursts can be triggered by an I^2C command. This automatically generates the modulated LED control signal for the integration phase of every image of a burst. The image data is transmitted over a MIPI D-PHY interface consisting of four differential data lanes and one differential clock lane. A MIPI CSI-2 receiver is required on the controller side to extract the image data from the stream. Based on the received data, distance and amplitude can then be computed for every pixel.

A separate safety illumination unit can be used to check the sensor operation based on optical input.

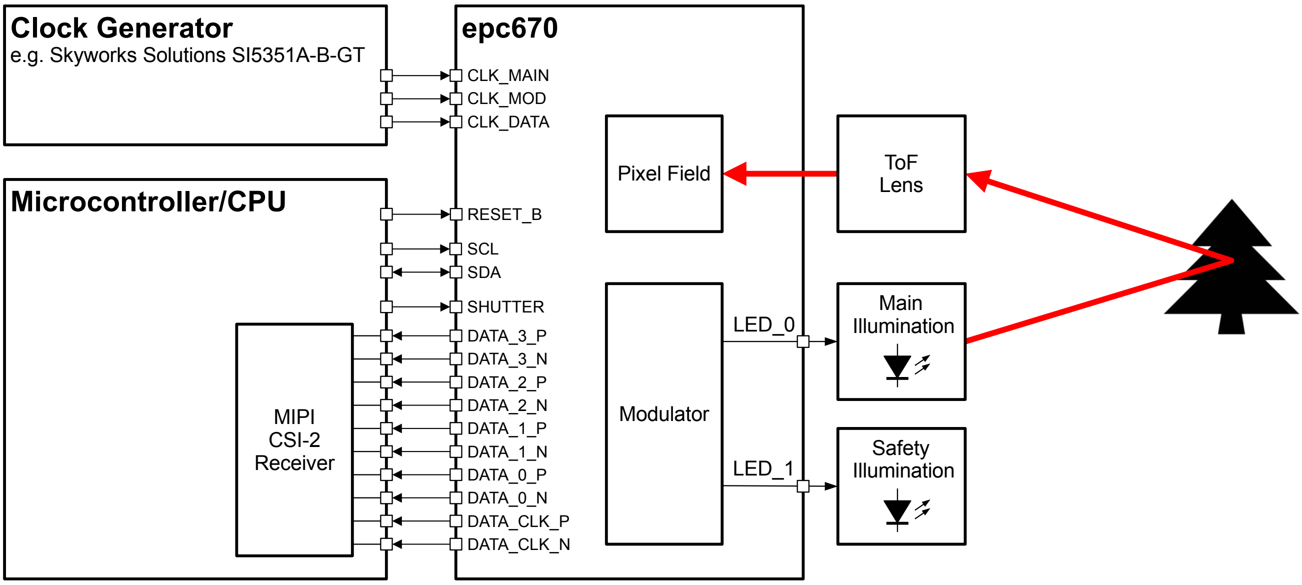


Figure 2: Typical application diagram

2. Main characteristics

All characteristics are at typical operational ratings, T_A = +25 °C, modulation frequency 10 MHz, supply voltages at nominal value, unless otherwise stated.

2.1. Optical characteristics

Table 1: Optical characteristics

Parameter	Description	Conditions/Comments	Value	Unit
Res	Resolution	Active pixels (default)	320 × 240	pixel
A_{PIXEL}	Pixel photosensitive area	100% fill factor	20 × 20	µm²
A_{SENSOR}	Pixel field area	Area of sensor array	6.4 × 4.8	mm²

2.2. Imaging characteristics

Table 2: Imaging characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
TOF sensitivity S_{TOF}	• Modulation frequency: 10 MHz • ToF amplitude: 1'500 LSB • CDS gain: 4 • Wave length: 940 nm	250	290	320	$\frac{pW/mm^2}{LSB}$
ToF amplitude PRNU	ToF amplitude photo response non-uniformity, @ 1000 LSB		4%		
DRNU	Distance response non-uniformity, @ 1'500 LSB, no compensation	50 (1)	250 (2)		mm
Distance noise (dark)	Temporal distance noise (1σ) without ambient light • ToF amplitude: 500 LSB (~21.5k e-) @ CDS gain 0.75	10 (1)	18	25	mm
I_{Dark}	Dark current @ CDS gain 4 (grayscale signal level increase during integration in the dark)		15	30	LSB/ms
SE	Shutter efficiency @ 940 nm wave length	98.0%	99.0%	99.5%	
PLS	Parasitic light sensitivity @ 940 nm wave length	0.5%	1.0%	2.0%	
S_{BW}	Grayscale sensitivity • 100 µs integration time • CDS gain: 4	80	90	100	$\frac{pW/mm^2}{LSB}$
DSNU	Dark signal non-uniformity @ CDS gain 0.75	15	20	30	LSB
PRNU	Photo response non-uniformity @ CDS gain 0.75		5%		

Notes:

1 Target for typical case

2 Diagonal distance shift across the pixel field

Figure 3 illustrates the dependence of the distance noise on the ToF amplitude.

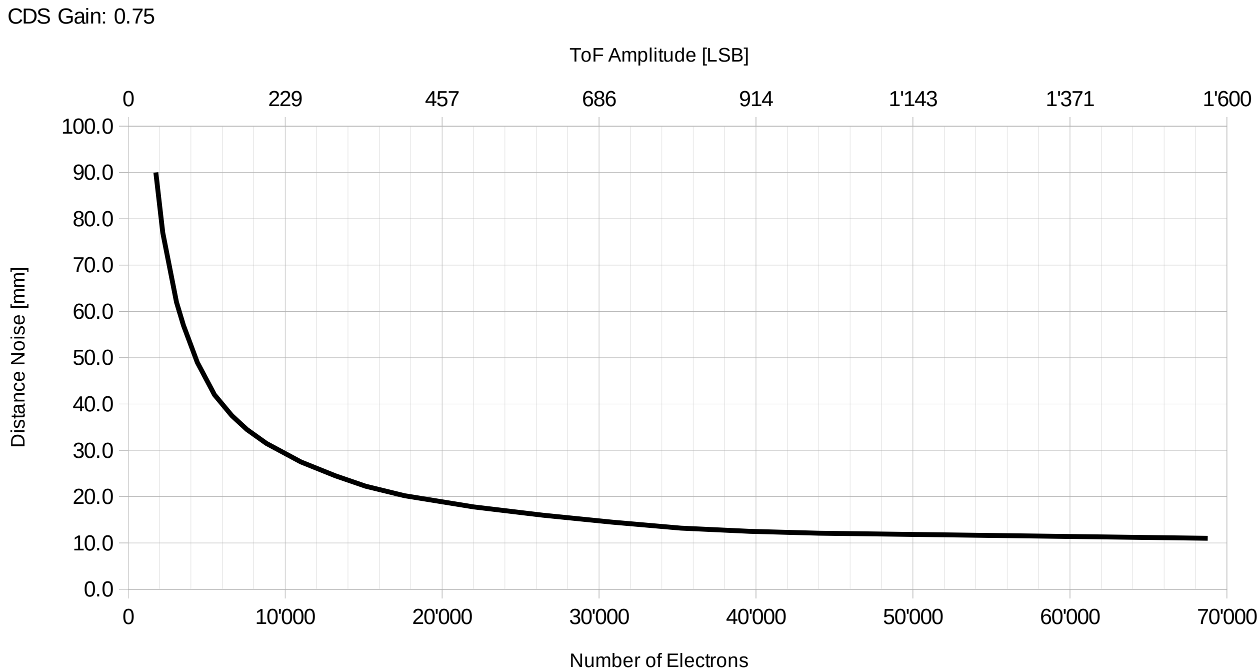


Figure 3: Distance noise vs. ToF amplitude without ambient light

2.3. Ambient light suppression (ABS)

An important function of the 3D TOF pixel is the ambient light suppression. It removes DC or low frequency modulated light caused by sunlight, room illumination, etc. from the modulated light generated by the camera illumination. The amount of collected ambient light is proportional to the integration time. The longer the integration time, the more unwanted light will be collected. It is good practice to keep the integration time for TOF imaging below 1 ms. In addition, the use of optical band-pass filters to block the unwanted spectrum of light is mandatory for outdoor applications.

Table 3: Ambient light suppression

Parameter	Description	Integration time	Wavelength	Typical value	Unit
$E_{e,max}$	Max. irradiance, DC light	100 µs	940 nm	60	µW/mm²
		800 µs	940 nm	7.5	µW/mm²
	Full well capacity of storage gates	n/a	n/a	5	Me^-
	Ambient light energy density at imager surface corresponding to full well capacity of storage gates	n/a	940 nm	6	nJ/mm²

2.4. Operating conditions and electrical characteristics

Table 4: Operating conditions and electrical characteristics

Parameter	Description	Conditions/Comments	Min.	Typ.	Max.	Unit
V_{DD_D}, V_{DD_PLL}	Digital supply voltage	Ripple (1) < ± 20 mV	1.71	1.80	1.98	V
$V_{DD\_A/CDS/COMP/TXG}$	Analog supply voltage (2)	Ripple (1) < ± 20 mV	4.9	5.0	5.1	V
V_{DD_PXH}	High voltage pixel driver supply voltage (2)	Ripple (1) < ± 20 mV	9.5	10	10.5	V
V_{DD_SF}	Source follower supply voltage	Noise shall be minimum.	9.5	10	10.5	V
$V_{DD\_FD\_RST}$	Floating diffusion reset supply voltage	Noise shall be minimum.	8.5	9	10	V
V_{BS}	Backside supply voltage		-20.0	-15.0	-14.5	V
I_{VDD_D}	Total digital supply current, including MIPI D-PHY supply currents		45	230	250	mA
I_{VDD_PLL}	PLL supply current	For both PLLs together	6	7	8	mA
$I_{VDD\_A/CDS/COMP/TXG}$	Analog supply current		80	225	250	mA
I_{VDD_PXH}	High voltage pixel driver supply current		0.25	0.30	0.35	mA
I_{VDD_SF}	Source follower supply current		11.0	12.5	14.0	mA
$I_{VDD\_FD\_RST}$	Floating diffusion reset supply current		< 1	< 1	< 1	mA
I_{VBS}	Backside supply current (3)		-20	-4.5	-2.9	mA
$I_{LED\_0/1}$	LED_0/1 output sink/source current (DC)				5	mA

Notes:

1 Min. and max. voltage values include noise and ripple voltages.

2 Voltage supplies have direct influence on measurement performance. They must be properly decoupled.

3 The current is increasing for more ambient light and it is further increasing the more negative the applied V_{BS} is.

2.5. Power consumption

The epc670 has several power states/levels during the different operation phases which are described in Table 5 and Figure 4.

Table 5: Typical average power consumption levels at different operating states

Power state	Power [mW]	Operation description
RESET	95	All supplies are powered-up and stable, RESET_B = 0, PLLs and all system clocks are not running
IDLE (STATIC)	745	RESET_B = 1, PLLs and all system clocks are running, waiting for shutter
INTEGRATION	1425	Image acquisition (active illumination and demodulation in pixel)
READOUT	1760	Integration finished, readout of pixel field, AD conversion and data transmission

Note: All the values in Table 5 are assuming a backside supply current I_{VBS} of 5 mA resulting in a contribution of 75 mW.

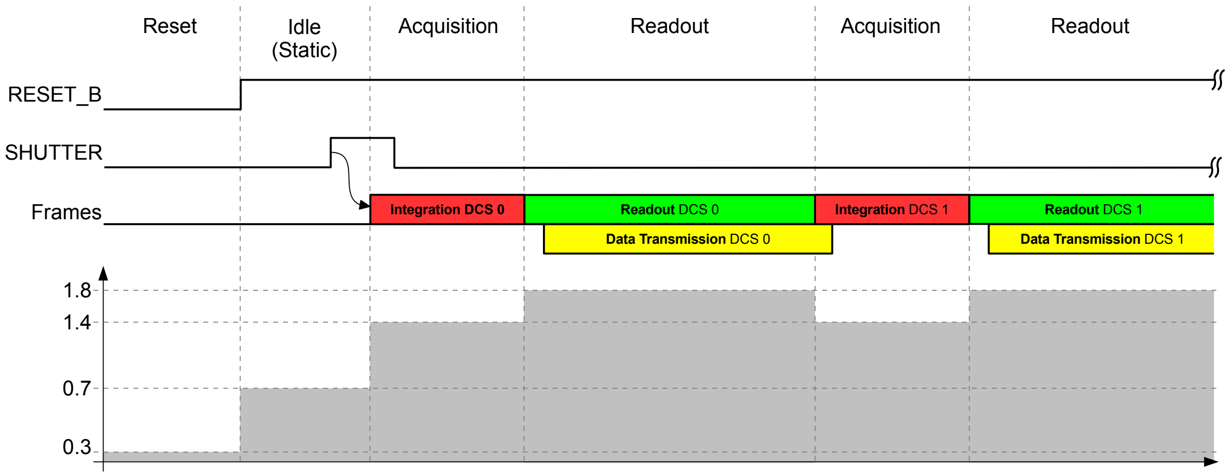


Figure 4: Power consumption levels for different operating states

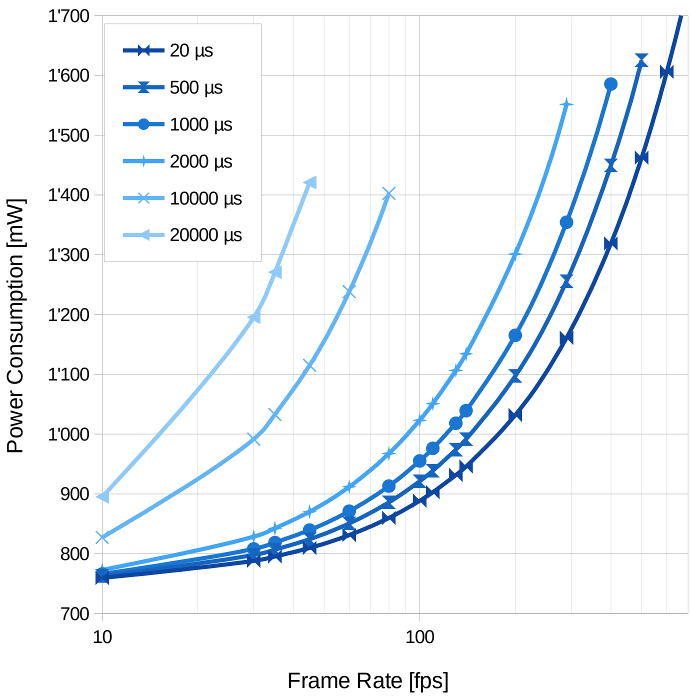


Figure 5: Typical average power consumption for static power control depending on DCS frame rate
(usually 4 DCSs per distance image)

2.6. Absolute maximum ratings

Table 6: Absolute maximum ratings

Parameter	Conditions
Supply voltage V_{DD_D}, V_{DD_PLL}	-0.5 V ... +2.0 V
Supply voltage V_{DD_A}, V_{DD_CDS}, V_{DD_COMP}, V_{DD_TXG}	-0.5 V ... +5.5 V
Supply voltage V_{DD_PXH}	-0.5 V ... +13.5 V
Supply voltage V_{BS}	-20.5 V ... +0.5 V
Voltage to any pin in the same V_{SC} supply class.	$V_{SC,min}$ - 0.3 V … $V_{SC,max}$ + 0.3 V
ESD rating	JEDEC HBM class 1C (1 kV to < 2 kV)
Junction temperature (T_J)	-40 °C to +125 °C
Relative humidity	0% ... 95%, non-condensing

2.7. Timing parameters

Table 7: Timing parameters

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
f_{CLK_MAIN}	Main clock input frequency			125	125	MHz
$t_{CLK\_MAIN\_jitter}$	Main clock input phase jitter	Peak-to-peak, cycle to cycle			50	ps
f_{CLK_DATA}	Data clock input frequency			125	125	MHz
$t_{CLK\_DATA\_jitter}$	Data clock input phase jitter	Peak-to-peak, cycle to cycle			50	ps
t_{reset}	Time for main chip reset (ad pad)	Supplies ramped up and stable	100			ns
$t_{startup}$	Start-up time			721		µs
t_{PLL}	PLL lock time				700	µs
t_{ADC_cal}	ADC gain calibration time	Following $t_{startup}$ in Normal Mode		342		µs
f_{CLK_MOD}	Modulation clock frequency (at pad)	LED modulation frequency = f_{CLK_MOD} / 4	0.4	40	125	MHz
f_{LED}	LED modulation frequency		0.1	10	31.25	MHz
$D_{unambiguity}$	Unambiguity distance		4.8	15	1'500	m
t_{DL_coarse}	Delay line resolution coarse	49 steps		2.1		ns
t_{DL_max}	Max. delay of the delay line				105	ns
d_{DL_max}	Max. virtual distance with the DL	$d_{DL\_max} = c \times t_{DL\_max} / 2$			15.75	m
f_{SCL}	I^2C data rate			400	1'000	kbit/s
t_{EEPROM_Write}	Time for EEPROM write access	Waiting time per byte			25	ms

2.8. Frame rate

Figure 6 illustrates the achievable DCS frame rate depending on the selected integration time. For short integration times, mainly the time required to read out the pixel field determines the achievable frame rate.

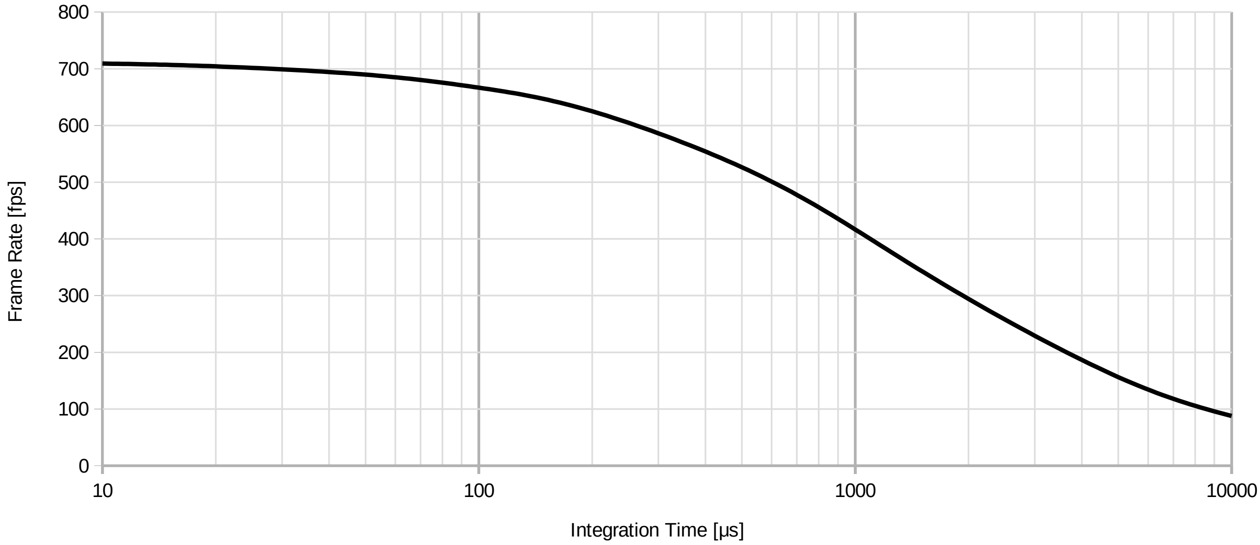


Figure 6: Achievable DCS frame rate based on integration time

2.9. Distance measurement temperature drift

The contributions of temperature effects on distance measurements are characterized in Table 8.

Table 8: Optical characteristics (10 MHz modulation frequency)

Parameter	Description	Conditions / Comments	Min.	Typ.	Max.	Unit
TC_{PIX}	Pixel	Valid up to 105 °C		20		mm/K
TC_{DL}	Delay line	Per coarse step		0.65		mm/K

2.10. Other characteristics

Table 9: Other characteristics

Parameter	Description	Conditions / Comments	Min.	Typ.	Max.	Unit
P_{Pk}	Power dissipation (average)	30 ToF fps, 1 ms integration time See Chapter 2.5 for more details.		1000		mW
R_{Th}	Thermal resistance	With solder balls and underfill, excl. PCB			1	K/W
T_{OP}	Operating temperature chip/circuitry		-40	60	125	°C
$T_{OP, optical}$	Optical performance temperature		-40	60	105	°C
Reliability	AEC-Q100 (upon request)	Grade 2	-40		125	°C
Environment	RoHS compliance			compliant		

3. Mechanical dimensions

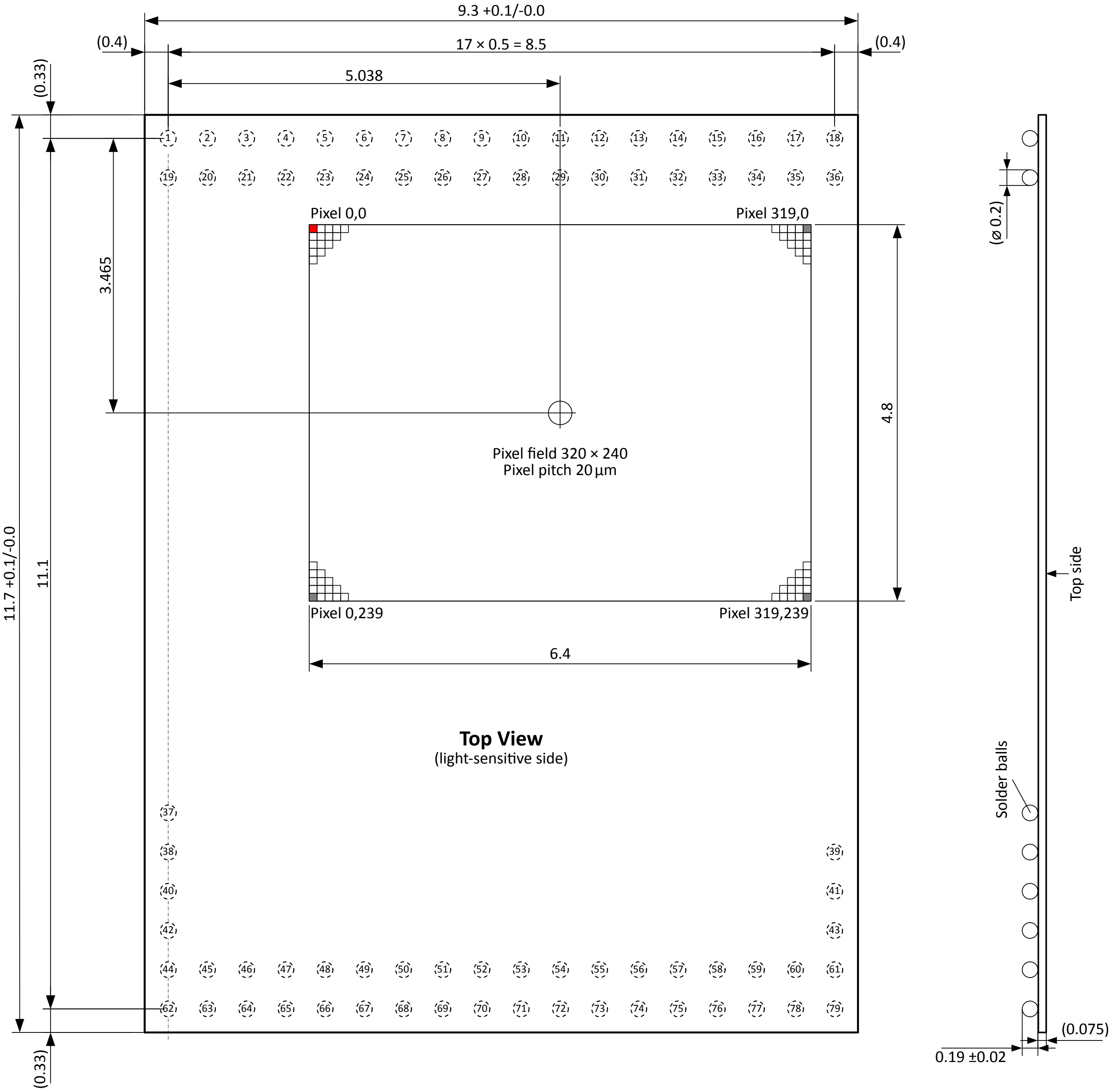
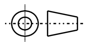


Figure 7: Mechanical dimensions (top view)

Notes:

- 
- All measures are in millimeters.
- Not specified tolerances: ±0.001 mm
- Dimensions in brackets are informal only.
- Top side is illumination side.
- Pin 37 is asymmetrical by purpose in order to allow location identification with a vision system during the SMT assembly process. It is highly recommended to check the orientation of pins 1 and 37.

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