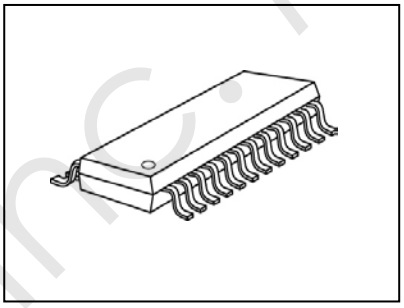
16-Channel PWM Constant Current LED Driver for 1:16 Time-Multiplexing Applications

Features



- 3V-5.5V supply voltage
- 16 constant current output channels
- Constant output current range:
  - 4~60mA @ V_{DD}=3.3~5V supply voltage
- Excellent output current accuracy:
  Between channels:：<±2.5%(Max.)
  Between ICs: <±3%(Max.)
- Built-in 8K-bit SRAM to support time-multiplexing for 1 ~ 16 scans
- 16/15/14/13-bit color depth PWM control to improve visual refresh rate
- 6-bit current gain，12.5%~100%
- LED failure isolation
  - LED failure induced cross elimination
  - Compulsory LED open detection
- Integrating ghost elimination circuit
- Built-in PWM enhancement
- Support double refresh mode
- GCLK multiplier technology
- Maximum data clock frequency: 15MHz@V_{DD}=5V

Product Description

MBI5262 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 16/15/14/13-bit color depth. MBI5262 features a 16-bit shift register which converts serial input data into each pixel's gray scale of the output port. Sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of V_F variations. The output current can be preset through an external resistor. The innovative architecture with embedded SRAM is designed to support up to 1:16 time-multiplexing applications. Users only need to send the whole frame data once and to store in the embedded SRAM of the LED driver, instead of sending every time when the scan line is changed. It helps to save the data bandwidth and to achieve high grayscale with very low data clock rate. With scan-type Scrambled-PWM (S-PWM) technology, MBI5262 enhances PWM by scrambling the "on" time of each scan line into several "on" periods and sequentially drives each scan line for a short "on" period. The enhancement equivalently increases the visual refresh rate of scan-type LED displays. In addition, the innovative GCLK multiplier technique doubles visual refresh rate.

MBI5262 drives the corresponding LEDs to the brightness specified by image data. With MBI5262, all output channels can be built with 14-bit color depth. When building a 14-bit color depth video, S-PWM technology reduces the flickers and improves the image fidelity.

Through compulsory error detection, MBI5262 detects individual LED for open-circuit errors without extra

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components. MBI5262 equipped an innovative cross elimination function, and it solves the cross phenomenon induced by failure LEDs. Besides, integrated ghost elimination and high contrast interference circuit eases the ghost problems and improve image contrast.

Block Diagram

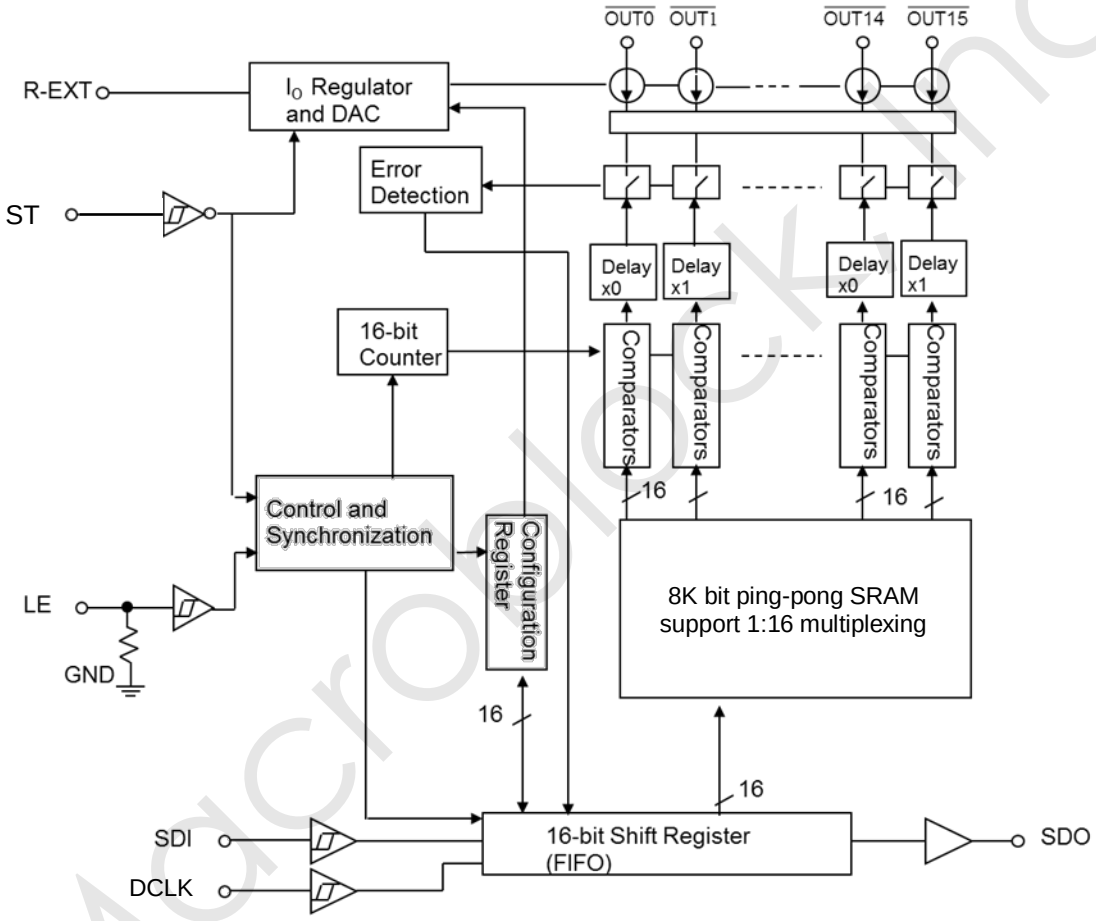
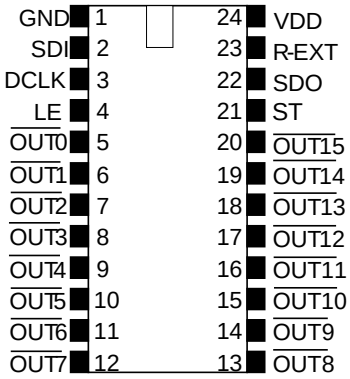


Figure 1

Pin Configuration



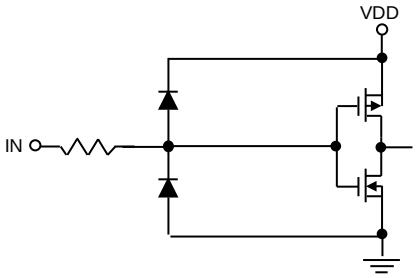
MBI5262GP

Terminal Description

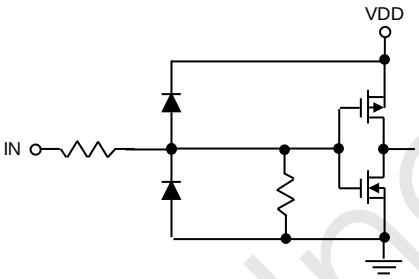
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$~$\overline{OUT15}$	Constant current output terminals
Scan toggle(ST)	Using PLL after driver finishes any scan display, driver will enter deadtime. After external toggle signal changes itself, driver will wait MT internal gclk, and then driver finish deadtime.
SDO	Serial-data output to the receiver-end SDI of next LED driver
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

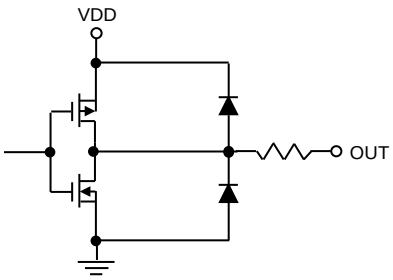
GCLK, DCLK, SDI terminal



LE Terminal



SDO Terminal



OUT0~15

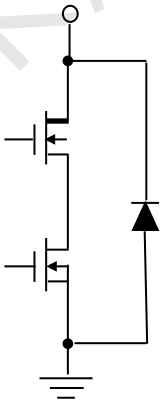


Figure 2

Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	3~5.5	V
Input Voltage(SDI, DCLK, LE, San toggle)		V_{IN}	-0.4 ~ V_{DD}+0.4	V
Output Current per Output Channel		I_{OUT}	+60	mA
Sustaining Voltage at OUT port		V_{DS}	-0.5 ~ V_{DD}+0.4	V
GND Terminal Current		I_{GND}	960	mA
Power Dissipation (On 4 Layer PCB, Ta=25°C)*	GP	P_D	1.079	W
Thermal Resistance (On 4 Layer PCB, Ta=25°C)*	GP	$R_{th(j-a)}$	69.5	°C/W
Junction Temperature		$T_{j,max}$	150**	°C
Operating Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	HBM (MIL-STD-883G Method 3015.7, Human Body Mode)	HBM	Class 3A (5KV)	
	MM (JEDEC EIA/JESD22-A115, Machine Mode)	MM	Class M4 (≧400V)	

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-	4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$	-	-	VLED+0.4	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"	4	-	60	mA
		I_{OH}	SDO	-	-	-1.0	mA
		I_{OL}	SDO	-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC	0.75xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC	GND	-	0.25xV_{DD}	V
Start Up Voltage		V_{STUP}	-		2.4		V
UVLO Voltage		V_{UVLO}	-		2.2		V
Output Leakage Current		I_{OH}	V_{DS}=VDD+0.4V	-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA	-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA	4.6	-	-	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=4~60mA, V_{DS}=1.0V, R_{ext}=960Ω	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=4~60mA, V_{DS}=1.0V, R_{ext}=960Ω	-	±1.5	±3	%
Open detection voltage		V_{open}	Open Code=[111]	-	2	-	V
			Open Code=[101]	-	1.37	-	V
			Open Code=[010]	-	1.0	-	V
			Open Code=[000]	-	0.5	-	V
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V,	-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.6V and 5.5V	-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE	-	100	-	KΩ
Supply Current (DCLK=GCLK =0Hz)	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off	-	10.2	11.5	mA
		I_{DD}(off) 2	R_{ext} =960Ω , $\overline{OUT0}$ ~ $\overline{OUT15}$=Off	-	14.2	15.5	mA
		I_{DD}(off) 3	R_{ext} =192Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off	-	24.2	24.5	mA
Supply Current (GCLK=20Hz)	"On"	I_{DD}(on) 2	R_{ext} =960Ω , $\overline{OUT0}$ ~ $\overline{OUT15}$=ON	-	14.2	15.5	mA
		I_{DD}(on) 3	R_{ext} =192Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=ON	-	24.2	24.5	mA

* One channel on.

Switching Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=960Ω V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	7	-	-	ns
	LE↑ – DCLK↑	t_{SU1}		10	-	-	ns
	LE↓(vsync/swrst) – GCLK	t_{SU2}		600			ns
	LE↓ – DCLK↑	t_{su3}***		15			ns
Hold Time	DCLK↑ - SDI	t_{H0}		8	-	-	ns
	DCLK↑ - LE	t_{H1}		10	-	-	ns
	GCLK – LE↓(vsync/swrst)	t_{H2}		-			ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	17	19	ns
	GCLK –$\overline{OUT2n}$*	t_{PD1}		-	4.8	5.3	ns
	LE – SDO	t_{PD2}**		-	-	-	ns
Pulse Width	LE	$t_{w(LE)}$		16			ns
Command to command		t_{cc}		52	-	-	ns
Data Clock Frequency		F_{DCLK}		2	-	20	MHz
Compulsory error detection operation time***		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	25	35	ns
Output Fall Time of Output Ports		t_{OF}		-	25	35	ns
Dead time		t_{dth}		600	-	-	ns

*Output waveforms have good uniformity among channels.
**In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.
***Users have to leave more time than the maximum error detection time for the error detection.

Electrical Characteristics (V_{DD}=4.6V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.2	4.6	5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	VLED+0.4	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		4	-	60	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.75xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.25xV_{DD}	V
Start Up Voltage		V_{STUP}	-			2.4		V
UVLO Voltage		V_{UVLO}	-			2.2		V
Output Leakage Current		I_{OH}	V_{DS}=VDD+0.4V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=4~60mA V_{DS}=1.0V	R_{ext}=960Ω	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=4~60mA V_{DS}=1.0V	R_{ext}=960Ω	-	±1.5	±3	%
Open detection voltage		V_{open}	Open Code=[111]		-	2	-	V
			Open Code=[101]		-	1.37	-	V
			Open Code=[010]		-	1.0	-	V
			Open Code=[000]		-	0.5	-	V
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V,		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.6V and 5.5V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		-	100		KΩ
Supply Current (DCLK=GCLK =0Hz)	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off			10.2	11.5	mA
		I_{DD}(off) 2	R_{ext} =960Ω , $\overline{OUT0}$ ~ $\overline{OUT15}$=Off			14.2	15.5	mA
		I_{DD}(off) 3	R_{ext} =192Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off			24.2	24.5	mA
Supply Current (GCLK=20Hz)	"On"	I_{DD}(on) 2	R_{ext} =960Ω , $\overline{OUT0}$ ~ $\overline{OUT15}$=ON			14.2	15.5	mA
		I_{DD}(on) 3	R_{ext} =192Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=ON			24.2	24.5	mA

* One channel on.

Switching Characteristics (V_{DD}=4.6V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	V_{DD}=4.6V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=960Ω V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	7	-	-	ns
	LE↑ – DCLK↑	t_{SU1}		10	-	-	ns
	LE↓(vsync/swrst) – GCLK	t_{SU2}		600			ns
	LE↓ – DCLK↑	t_{su3}***		15			ns
Hold Time	DCLK↑ - SDI	t_{H0}		8	-	-	ns
	DCLK↑ - LE	t_{H1}		10	-	-	ns
	GCLK – LE↓(vsync/swrst)	t_{H2}		-			ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	17	19	ns
	GCLK –$\overline{OUT2n}$*	t_{PD1}		-	4.8	5.3	ns
	LE – SDO	t_{PD2}**		-	-	-	ns
Pulse Width	LE	$t_{w(LE)}$		16			ns
Command to command		t_{cc}		52	-	-	ns
Data Clock Frequency		F_{DCLK}		2	-	20	MHz
Compulsory error detection operation time***		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	25	35	ns
Output Fall Time of Output Ports		t_{OF}		-	25	35	ns
Dead time		t_{dth}		600	-	-	ns

*Output waveforms have good uniformity among channels.
**In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.
***Users have to leave more time than the maximum error detection time for the error detection.

Electrical Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	VLED+0.4	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		4	-	60	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.75xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.25xV_{DD}	V
Start Up Voltage		V_{STUP}	-			2.4		V
UVLO Voltage		V_{UVLO}	-			2.2		V
Output Leakage Current		I_{OH}	V_{DS}=VDD+0.4V		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
		V_{OH}	I_{OH}=-1.0mA		4.6	-	-	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=4~60mA V_{DS}=1.0V	R_{ext}=960Ω	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=4~60mA V_{DS}=1.0V	R_{ext}=960Ω	-	±1.5	±3	%
Open detection voltage		V_{open}	Open Code=[111]		-	2	-	V
			Open Code=[101]		-	1.37	-	V
			Open Code=[010]		-	1.0	-	V
			Open Code=[000]		-	0.5	-	V
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V,		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 4.6V and 5.5V		-	±1.0	±2.0	% / V
Pull-down Resistor		R_{IN}(down)	LE		-	100		KΩ
Supply Current (DCLK=GCLK =0Hz)	"Off"	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off			10.2	11.5	mA
		I_{DD}(off) 2	R_{ext} =960Ω , $\overline{OUT0}$ ~ $\overline{OUT15}$=Off			14.2	15.5	mA
		I_{DD}(off) 3	R_{ext} =192Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=Off			24.2	24.5	mA
Supply Current (GCLK=20Hz)	"On"	I_{DD}(on) 2	R_{ext} =960Ω , $\overline{OUT0}$ ~ $\overline{OUT15}$=ON			14.2	15.5	mA
		I_{DD}(on) 3	R_{ext} =192Ω, $\overline{OUT0}$ ~ $\overline{OUT15}$=ON			24.2	24.5	mA

* One channel on.

Test Circuit for Electrical Characteristics

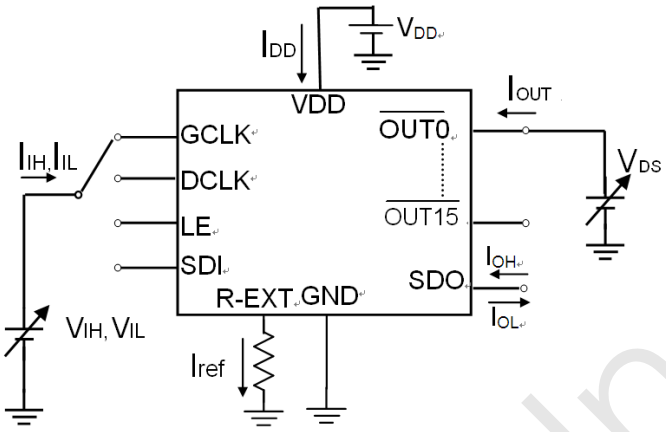


Figure 3

Switching Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=960Ω V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	7	-	-	ns
	LE↑ – DCLK↑	t_{SU1}		10	-	-	ns
	LE↓(vsync/swrst) – GCLK	t_{SU2}		600			ns
	LE↓ – DCLK↑	t_{su3}***		15			ns
Hold Time	DCLK↑ - SDI	t_{H0}		8	-	-	ns
	DCLK↑ - LE	t_{H1}		10	-	-	ns
	GCLK – LE↓(vsync/swrst)	t_{H2}		-	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	17	19	ns
	GCLK –$\overline{OUT2n}$*	t_{PD1}		-	4.8	5.3	ns
	LE – SDO	t_{PD2}**		-	-	-	ns
Pulse Width	LE	$t_{w(LE)}$		16	-	-	ns
Command to command		t_{cc}		52	-	-	ns
Data Clock Frequency		F_{DCLK}		2	-	20	MHz
Compulsory error detection operation time***		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	25	35	ns
Output Fall Time of Output Ports		t_{OF}		-	25	35	ns
Dead time		t_{dth}		600	-	-	ns

*Output waveforms have good uniformity among channels.
**In timing of "configuration read", the next DCLK rising edge should be t_{PD2} after LE's falling edge.
***Users have to leave more time than the maximum error detection time for the error detection.

Test Circuit for Switching Characteristics

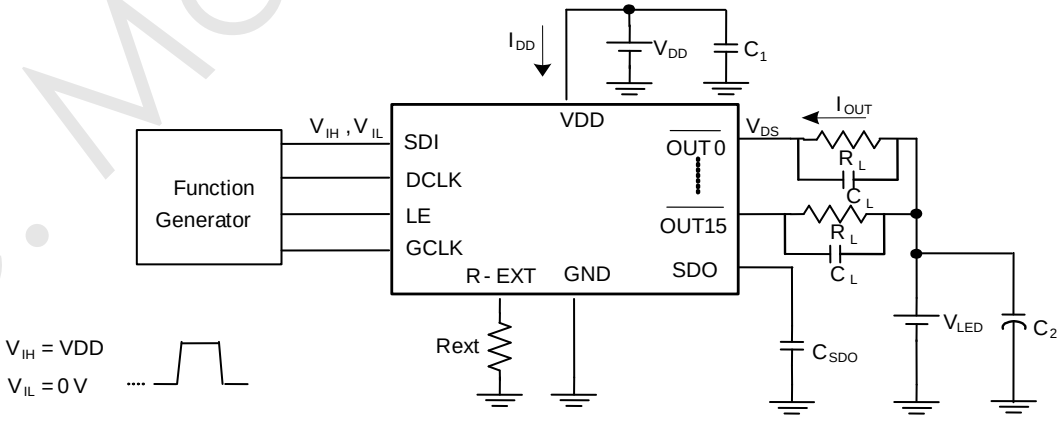
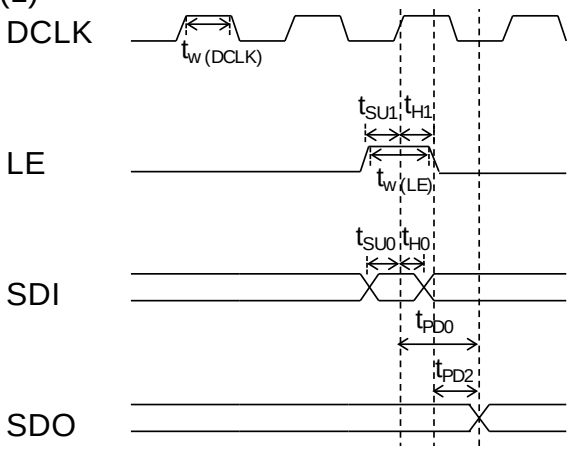


Figure 4

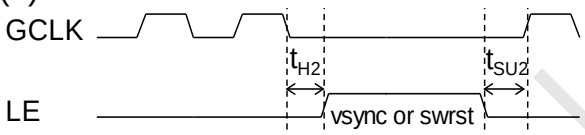
Timing waveform

◆ Control timing

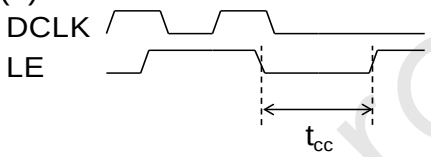
(1)



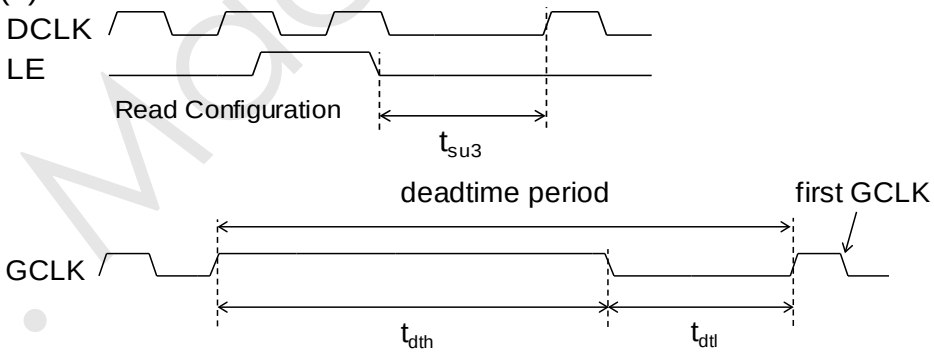
(2)



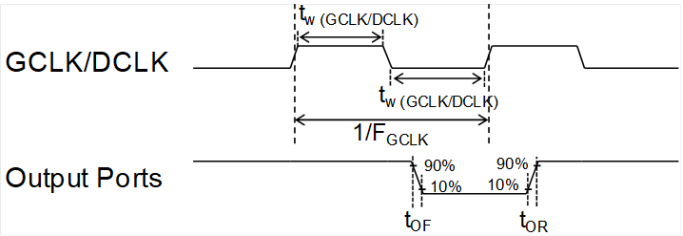
(3)



(4)



◆ Output timing

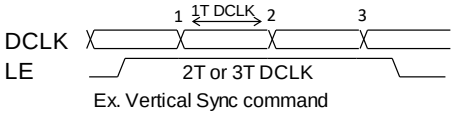


Control Command

Command Name	Signals Combination		Description
	LE	The Sum of DCLK Rising and Falling Edge Number when LE is asserted	The Action after a Falling Edge of LE
Stop Compulsory Error Detection	High	1	Stop compulsory error detection
Individual Latch	High	1	Serial data are transferred to the buffers
Vertical Sync	High	2 or 3	Display frame will be updated
Write Global Configuration 1-1*	High	4	Serial data are transferred to “Global Configuration 1-1 ”
Write Global Configuration 1-2*	High	5	Serial data are transferred to “Global Configuration 1-2 ”
Write Global Configuration 1-3*	High	6	Serial data are transferred to “Global Configuration 1-3 ”
Write Global Configuration 2-1*	High	7	Serial data are transferred to “Global Configuration 2-1 ”
Write Global Configuration 2-2*	High	8	Serial data are transferred to “Global Configuration 2-2 ”
Write Global Configuration 2-3*	High	9	Serial data are transferred to “Global Configuration 2-3 ”
Write Global Configuration 3-1*	High	10	Serial data are transferred to “Global Configuration 3-1 ”
Write Global Configuration 3-2*	High	11	Serial data are transferred to “Global Configuration 3-2 ”
Write Global Configuration 3-3*	High	12	Serial data are transferred to “Global Configuration 3-3 ”
Confirm Command	High	13	Confirm command needs to be sent before “write configure, enable/disable all outputs” commands.
Write Channel Configuration 1-1*	High	14	Serial data are transferred to “Channel Configuration 1-1 ”
Write Channel Configuration 1-2*	High	15	Serial data are transferred to “Channel Configuration 1-2 ”
Write Channel Configuration 1-3*	High	16	Serial data are transferred to “Channel Configuration 1-3 ”
Write Channel Configuration 2-1*	High	17	Serial data are transferred to “Channel Configuration 2-1”
Write Channel Configuration 2-2*	High	18	Serial data are transferred to “Channel Configuration 2-2 ”
Write Channel Configuration 2-3*	High	19	Serial data are transferred to “Channel Configuration 2-3 ”
Write Channel Configuration 3-1*	High	20	Serial data are transferred to “Channel Configuration 3-1 ”
Write Channel Configuration 3-2*	High	21	Serial data are transferred to “Channel Configuration 3-2 ”
Write Channel Configuration 3-3*	High	22	Serial data are transferred to “Channel Configuration 3-3 ”
Software Reset	High	26	Reset all digital circuit, but not include configure registers
Write Global Configuration 5-1*	High	30	Serial data are transferred to “Global Configuration 5-1 ”
Write Global Configuration 5-2*	High	31	Serial data are transferred to “Global Configuration 5-2 ”
Write Global Configuration 5-3*	High	32	Serial data are transferred to “Global Configuration 5-3 ”
Compulsory Error Detection (Open Error)	High	37	Start compulsory open error detection
Wake-up	High	43	Force IC leaving Chip Sleep Mode
Hardware Reset	High	63	Reset all digital circuit and configure registers

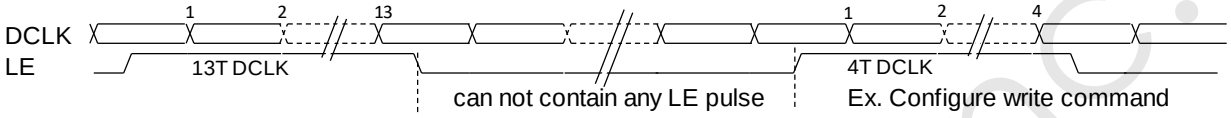
*Those commands can only be sent after “confirm command”**.**

- **Command which not need "Confirm Command" ahead**
  (Note: "T" means the numbers of DCLK rising and falling edge trigger)

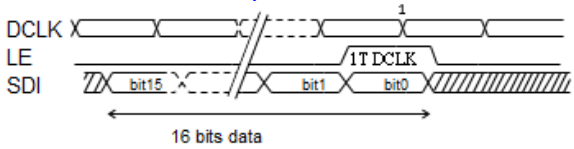


Ex. Vertical Sync command

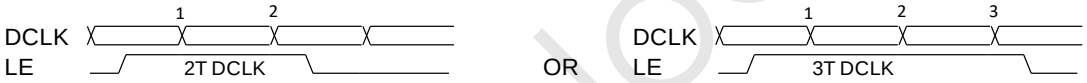
- **Command which need "Confirm Command" ahead**
  (Note: "T" means the numbers of DCLK rising and falling edge trigger)



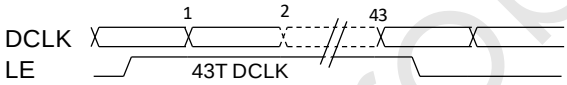
- Individual Latch (Note: "T" means the numbers of DCLK rising and falling edge trigger)



- Vertical Sync (Note: "T" means the numbers of DCLK rising and falling edge trigger)



- Wake-Up (Note: "T" means a rising or falling edge number of DCLK)



Definition of 1-1 Global Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F~B	Read/Write	Reserved	00 (Default)	Reserved
A~7	Read/Write	Number of Scan Line	4'h00 ~ 4'h03 (Default) ~ 4'h5F	Total Scan Lines (N_{line}) = Global cfg1-1[A:7] + 1
6~5	Read/Write	S-PWM Mode	2'h0 (Default)	16 bit
			2'h1	15 bit
			2'h2	14 bit
			2'h3	13 bit
4	Read/Write	Reserved	0 (Default)	Reserved
3~2	Read/Write	Refresh Rate/GCLK Number Per Scan (N_{GCLK})	2'h0 (Default)	Refresh Rate = 960 and GCLK number per scan = N_{GCLK} (1) SPWM mode=16bit, N_{GCLK} =4096 (Default) (2) SPWM mode=15bit, N_{GCLK} =2048 (3) SPWM mode=14bit, N_{GCLK} =1024 (4) SPWM mode=13bit, N_{GCLK} =512
			2'h1	Refresh Rate = 1920 and GCLK number per scan = N_{GCLK} (1) SPWM mode=16bit, N_{GCLK} =2048 (2) SPWM mode=15bit, N_{GCLK} =1024 (3) SPWM mode=14bit, N_{GCLK} =512 (4) SPWM mode=13bit, N_{GCLK} =256
			2'h2	Refresh Rate = 3840 and GCLK number per scan = N_{GCLK} (1) SPWM mode=16bit, N_{GCLK} =1024 (2) SPWM mode=15bit, N_{GCLK} =512 (3) SPWM mode=14bit, N_{GCLK} =256 (4) SPWM mode=13bit, N_{GCLK} =128
			2'h3	Reserved
1~0	Read/Write	Reserved	2'h0 (Default) ~ 2'h3	Reserved

Default setting of configuration register is 16'h0300

Definition of 1-2 Global Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	1	0	1	0	1	0	0	0

Bit	Attribute	Definition	Value	Function
F	Read/Write	Reserved	0 (Default)	Reserved
E~A	Read/Write	Reserved	5'h00 (Default) ~ 5'h1F	Reserved
9~0	Read/Write	Reserved	10'h000 ~ 10'h0A8 (Default) ~ 10'h3FF	Reserved

Default setting of configuration register is 16'h00A8

Definition of 1-3 Global Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0

Bit	Attribute	Definition	Value	Function
F~B	Read/Write	Reserved	00000 (Default)	Reserved
A~9	Read/Write	Reserved	00 (Default)	Reserved
8~0	Read/Write	Reserved	8'h00 ~ 8'hA8 (Default) ~ 8'hFF	Reserved

Default setting of configuration register is 16'00A8

Definition of 2-1 Global Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Attribute	Definition	Value	Function
F~D	Read/Write	Reserved	3'h0 (Default) ~ 3'h7	Reserved
C~A	Read/Write	Reserved	3'h0 (Default) ~ 3'h7	Reserved
9~8	Read/Write	Reserved	2'h0 (Default) ~ 2'h3	Reserved
7	Read/Write	Reserved	0 (Default)	Reserved
6	Read/Write	Reserved	0 (Default)	Reserved
5~3	Read/Write	Reserved	0 (Default)	Reserved
2~0	Read/Write	Reserved	2'h0 ~ 2'h2 (Default) ~ 2'h3	Reserved

Default setting of configuration register is 16'h0002

Definition of 2-2 Global Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	0	1	1	0	1	1	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F	Read/Write	Reserved	0 (Default)	Reserved
E	Read/Write	Reserved	1 (Default)	Reserved
D~C	Read/Write	Reserved	2'h0 ~ 2'h3 (Default)	Reserved
B~7	Read/Write	Reserved	5'h02 ~ 5'h06 (Default) ~ 5'h1F	Reserved
6~0	Read/Write	Reserved	7'h10 ~ 7'h60 (Default) ~ 7'h7F	Reserved

Default setting of configuration register is 16'h7360

Definition of 2-3 Global Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F	Read/Write	Data reset	0 (Default)	0: Disable 1: Enable
E~D	Read/Write	Internal GCLK Mode	00 (Default)	00: Disable 01: Enable 10~11: Reserved
C	Read/Write	Reserved	0 (Default)	Reserved
B~A	Read/Write	Reserved	2'h0 (Default) ~ 2'h3	Reserved
9~8	Read/Write	Reserved	2'h0 ~ 2'h3 (Default)	Reserved
7	Read/Write	Reserved	0 (Default)	Reserved
6	Read/Write	Reserved	0 (Default)	Reserved
5	Read/Write	Reserved	0 (Default)	Reserved
4	Read/Write	Reserved	0 (Default)	Reserved
3	Read/Write	Reserved	0 (Default)	Reserved
2	Read/Write	Reserved	0 (Default)	Reserved
1	Read/Write	Power saving mode 1	0 (Default)	0: Disable 1: Enable
0	Read/Write	Power saving mode 2	0 (Default)	0: Disable 1: Enable

Default setting of configuration register is 16'h0300

Definition of 3-1 Global Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F~0	Read/Write	Reserved	16'h0 (Default)	Reserved

Default setting of configuration register is 16'h0000

Definition of 3-2 Global Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F~E	Read/Write	Reserved	2'h0 ~ 2'h3 (Default)	Reserved
D	Read/Write	Reserved	0 (Default)	Reserved
C	Read/Write	Reserved	0 (Default)	Reserved
B	Read/Write	Reserved	0 (Default)	Reserved
A	Read/Write	Reserved	0 (Default)	Reserved
9~0	Read/Write	Reserved	10'h000(Default) ~ 10'h3FF	Reserved

Default setting of configuration register is 16'hC000

Definition of 3-3 Global Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F~0	Read/Write	Reserved	16'h0000 (default) ~ 16'hffff	Reserved

Default setting of configuration register is 16'h0000

Definition of 1-1 Channel Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Attribute	Definition	Value	Function
F	Read/Write	Ghosting effect elimination	0(default)	0:Disable 1:Enable
E~A	Read/Write	Ghosting effect elimination level setting 1	00000 ~ 11111(default)	00000: Disable 00001: Level 1 00010: Level 2 … 11111: Level 31
9~5	Read/Write	Ghosting effect elimination level setting 2	00000 ~ 11111(default)	00000: Disable 00001: Level 1 00010: Level 2 … 11111: Level 31
4~0	Read/Write	Ghosting effect elimination level setting 3	00000 ~ 11111(default)	00000: Disable 00001: Level 1 00010: Level 2 … 11111: Level 31

Default setting of configuration register is 16'h7FFF

Definition of 1-2 Channel Configuration Register

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Attribute	Definition	Value	Function
F	Read/Write	Ghosting effect elimination and gradient transition optimization in display channels	0(default)	0:Dsable 1:Enable
E~A	Read/Write	Gradient transition optimization in display channels voltage level setting 1	00000 ~ 11111(default)	00000: Disable 00001: Level 1 00010: Level 2 … 11111: Level 31
9~5	Read/Write	Gradient transition optimization in display channels voltage level setting 2	00000 ~ 11111(default)	00000: Disable 00001: Level 1 00010: Level 2 … 11111: Level 31
4~0	Read/Write	Gradient transition optimization in display channels voltage level setting 3	00000 ~ 11111(default)	00000: Disable 00001: Level 1 00010: Level 2 … 11111: Level 31

Default setting of configuration register is 16'h7FFF

Number of Scan Line

MBI5262 supports 1 to 16 scan lines. Please set the configuration register1 bit [C:8], according to the application.

Gray Scale Mode and Scan-type S-PWM

MBI5262 provides a selectable 14-bit or 13-bit gray scale by setting the configuration register1 bit [6:5]. The default value is set to '0' for 14-bit color depth. In 14-bit gray scale mode, users should still send 16-bit data with 2-bit '0' in LSB bits. For example, {14'h1234, 2'h0}.

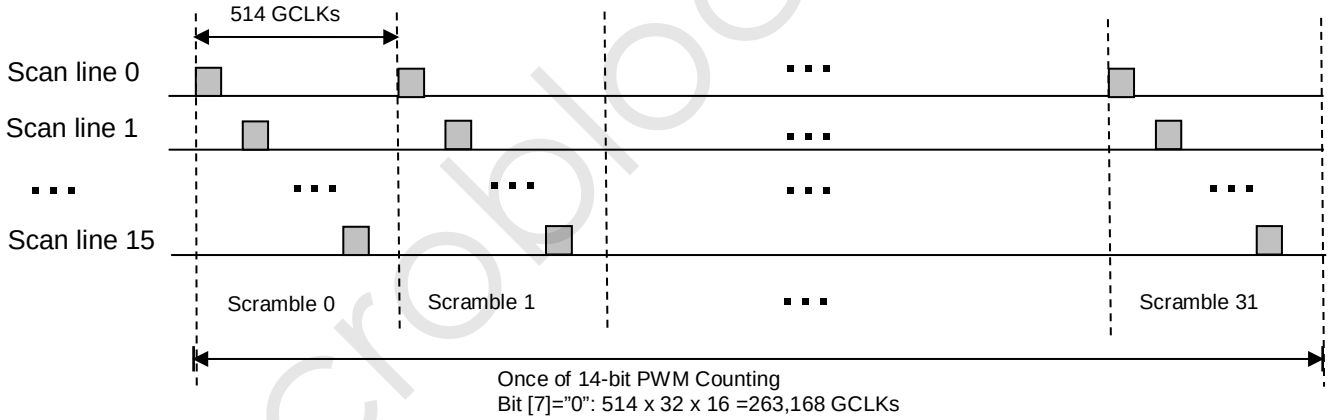
MBI5262 has a smart S-PWM technology for scan type. With S-PWM, the total PWM cycles can be broken into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles. The MSB information can be broken down into many refresh cycles to achieve overall same high bit resolution.

GCLK multiplier

MBI5262 provides a GCLK multiplier function by setting the configuration register1 bit [6]. The default value is set to '0' for GCLK multiplier disable.

GCLK multiplier disabled (configuration register1 bit [6] = 0)

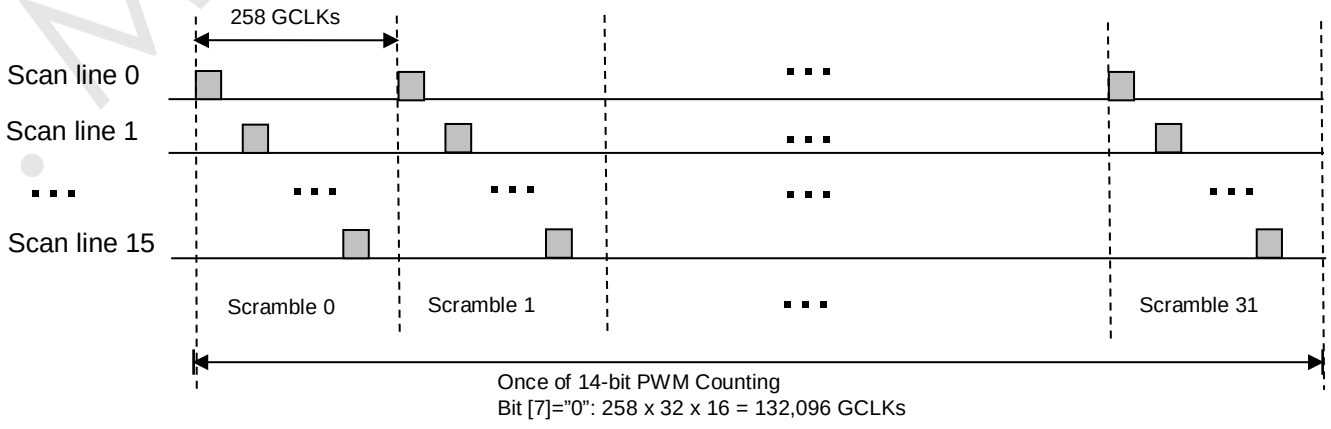
Display sequence of 32 scrambles



: Output ports are turned "on".

GCLK multiplier enabled (configuration register1 bit [6] = 1)

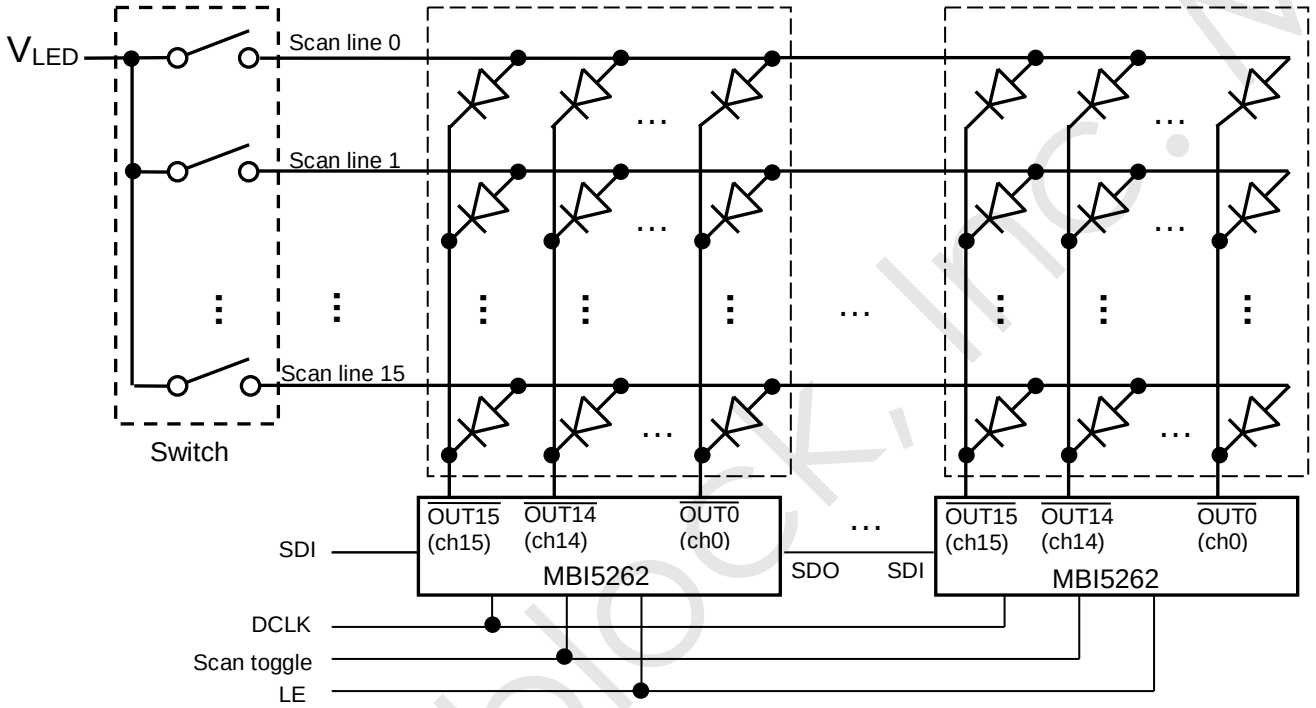
Display sequence of 32 scrambles



: Output ports are turned "on".

Operation Principal

Scan type application structure



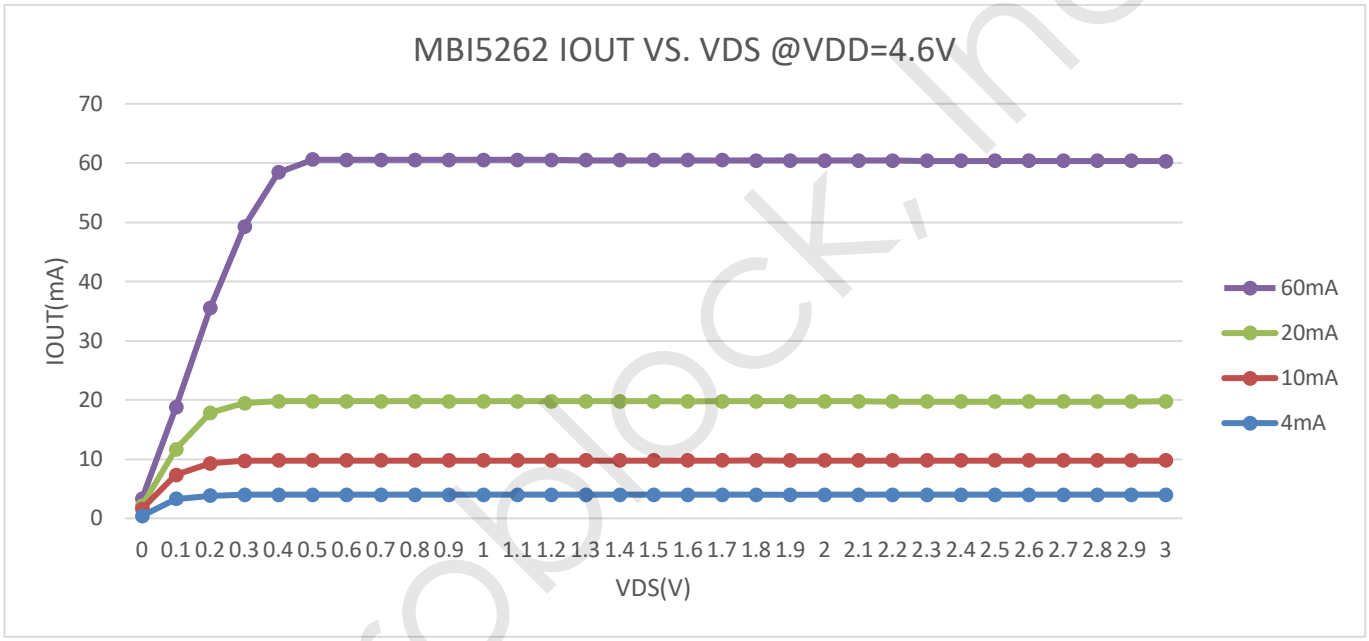
The above figure shows the suggested application structure of scan type scheme with 16 scan lines. The gray-scale data are sent by pin “SDI and SDO” with the commands formed by pin “LE” and “DCLK”. The output ports from 16 channels (OUT1~OUT15) will output the PWM result for each scan line at different time, so there must be one “Switch” to multiplex for each scan line. The switching sequence and method and the command usage will be described in the application note.

Constant Current

In LED display application, MBI5262 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

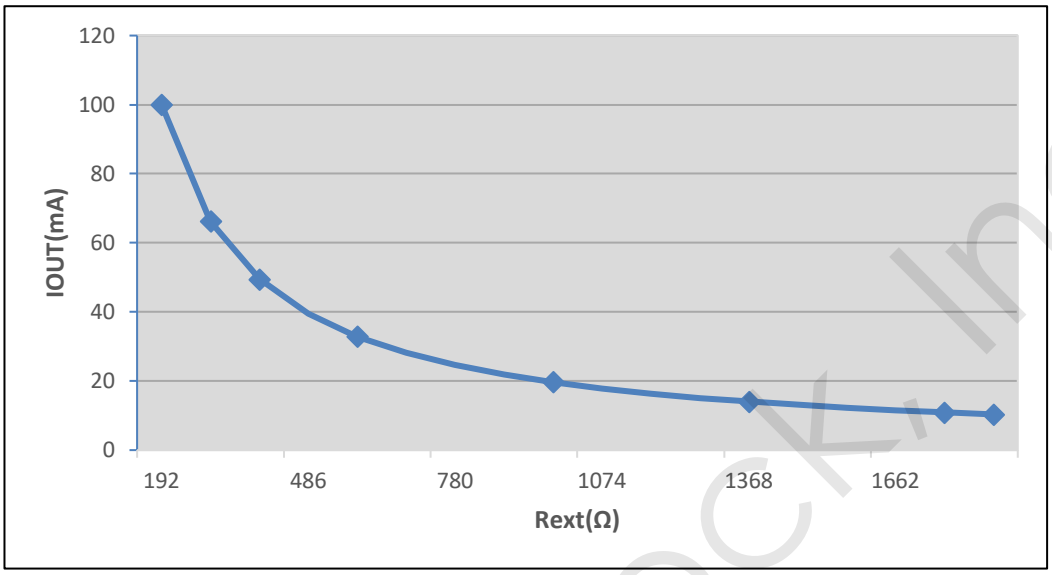
1) The maximum current variation between channels is less than 2.5%, and that between ICs is less than ±3%

2) In addition, the current characteristic of output stage is flat and user can refer to the figure below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.



Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.



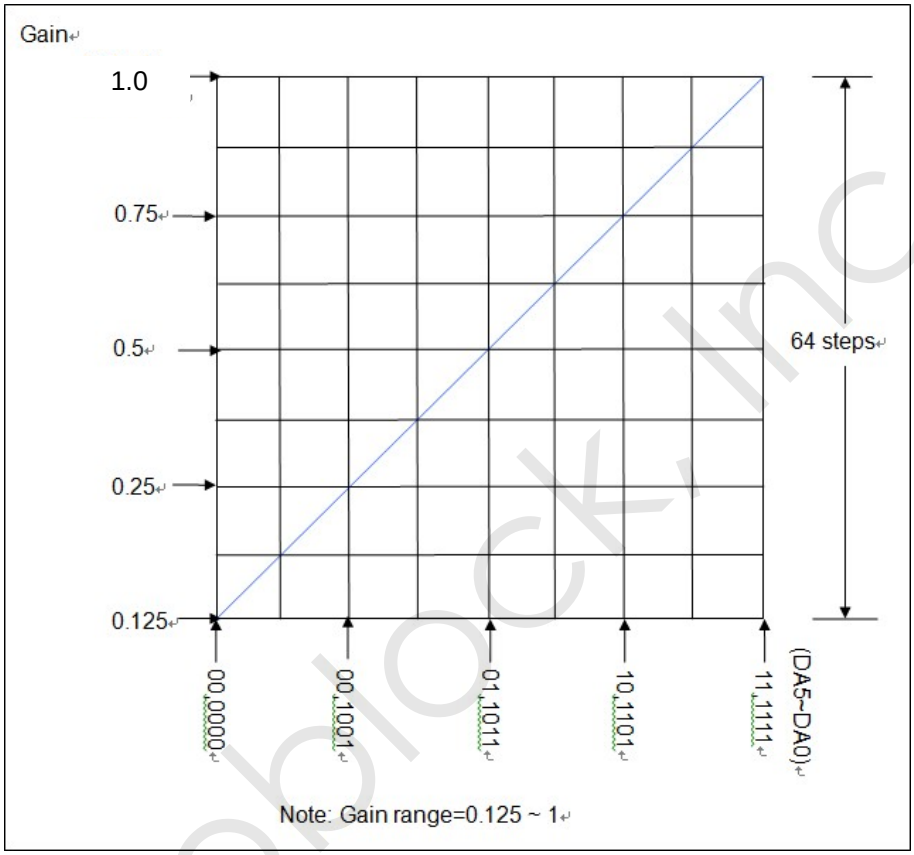
Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$ = 0.8Volt; I_{OUT} = ($V_{R\text{-}EXT}$ / R_{ext}) x 24 x G

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit 5 to bit 0 of the configuration register. The default value of G is 1. For your information, the output current is about 20mA when R_{ext}=700Ω if G is set to default value 1.

The formula and the setting for G are described in the next section.

Current Gain Adjustment



The 6 bits (bit 5~bit 0) of the configuration register set the gain of output current, i.e., G. As total 6-bit in number, i.e., ranged from 6'b000000 to 6'b111111, these bits allow the user to set the output current gain up to 64 levels. These bits can be further defined inside configuration register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	DA5	DA4	DA3	DA2	DA1	DA0

1. Bit 5 to bit 0 are DA5 ~ DA0.

The relationship between these bits and current gain G is:

$G=0.125+(D/63)x0.875$

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D= DA5x2^5+DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$

In other words, these bits can be looked as 6-bit mantissa DA5~DA0.

For example,

G=0.5, D=(0.5-0.125)/0.875x63=27

the D in binary form would be:

$D=27=0x2^5+1x2^4+1x2^3+0x2^2+1x2^1+1x2^0$

The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b011011

Package Power Dissipation (P_D)

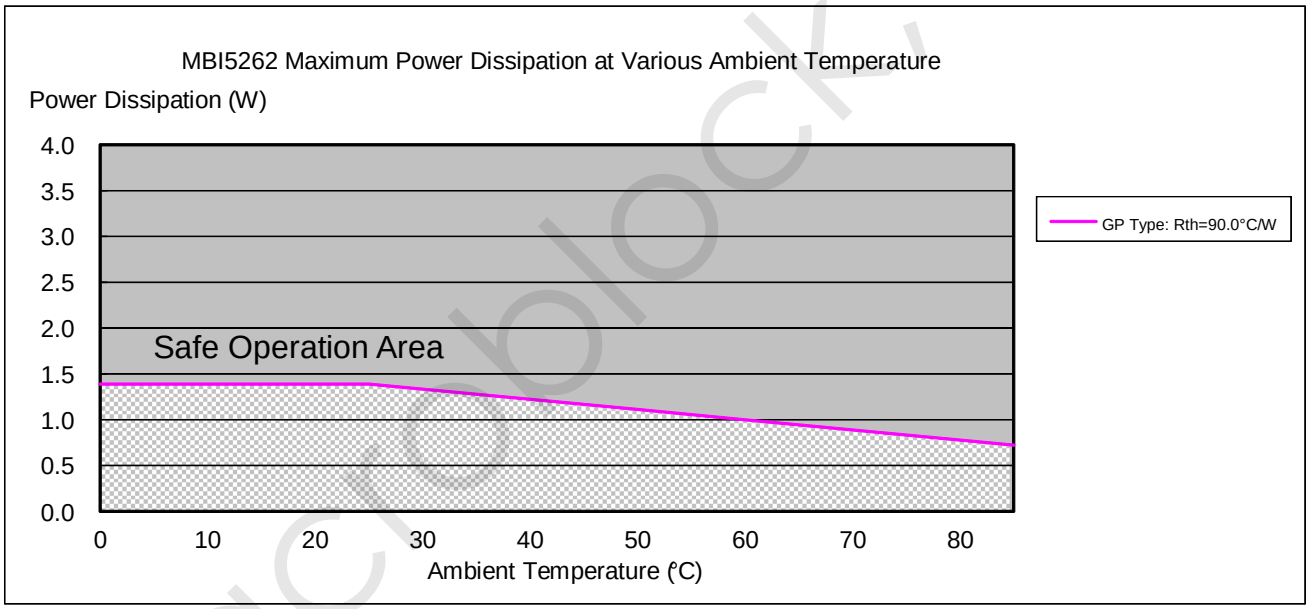
The maximum allowable package power dissipation is determined as $P_D(max)=(T_j–T_a)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep P_D (act)≤P_D (max), the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(T_j–T_a)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}$ /Duty/16, where T_j=150°C.

Please see the follow table for P_D and $R_{th(j-a)}$ for different packages:

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GP	90	1.38

The maximum power dissipation, $P_D(max)=(T_j–T_a)/R_{th(j-a)}$, decreases as the ambient temperature increases.



LED Supply Voltage (V_{LED})

MBI5262 is designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=1~20mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

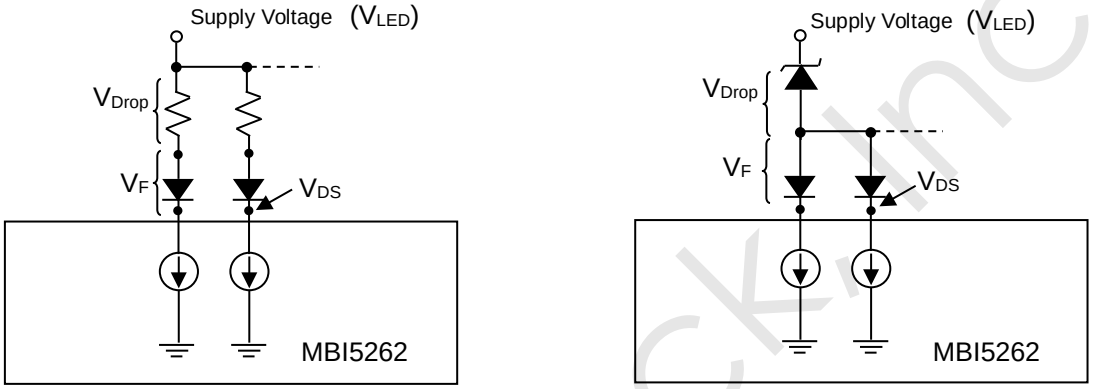


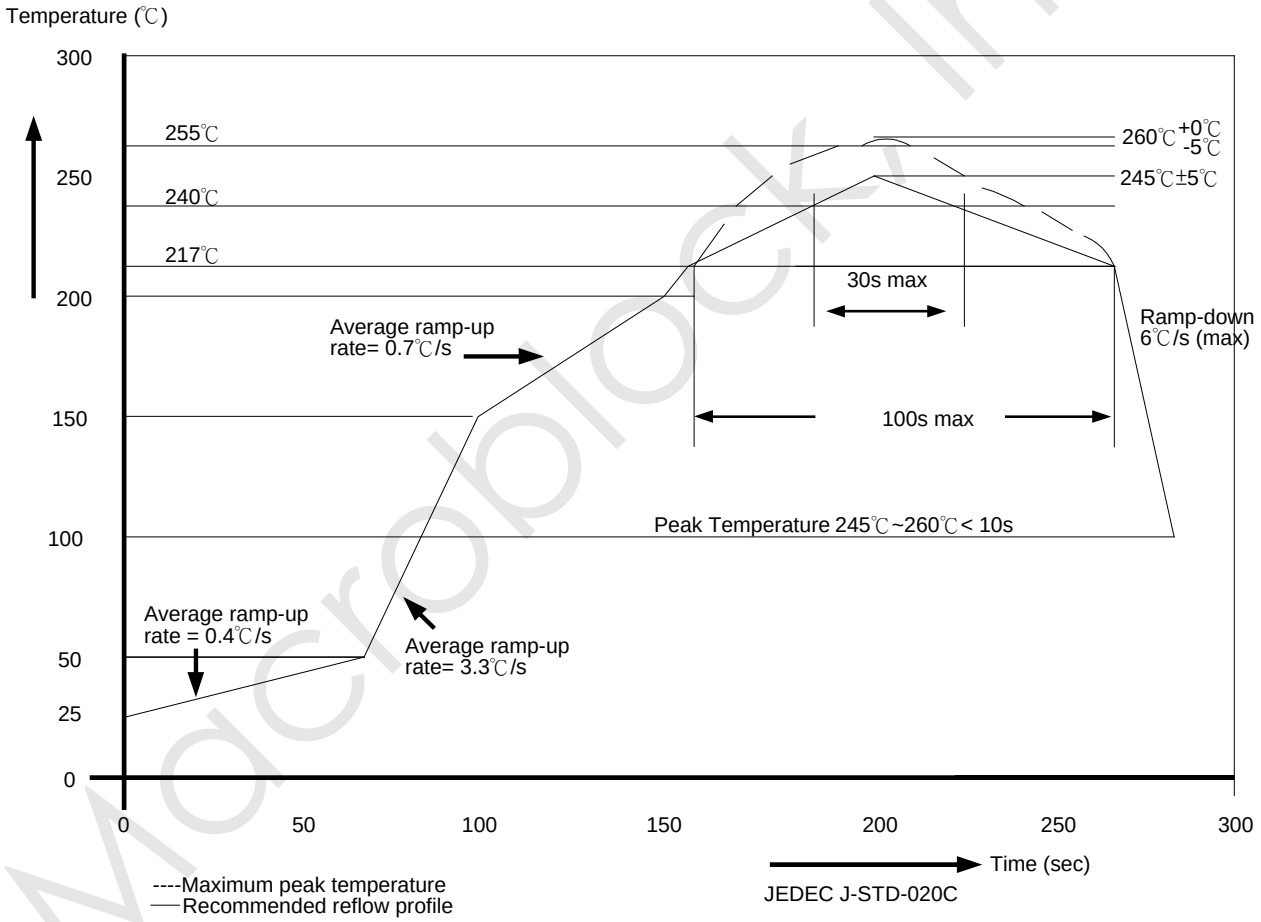
Figure 5

Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

Soldering Process of "Pb-free & Green" Package Plating*

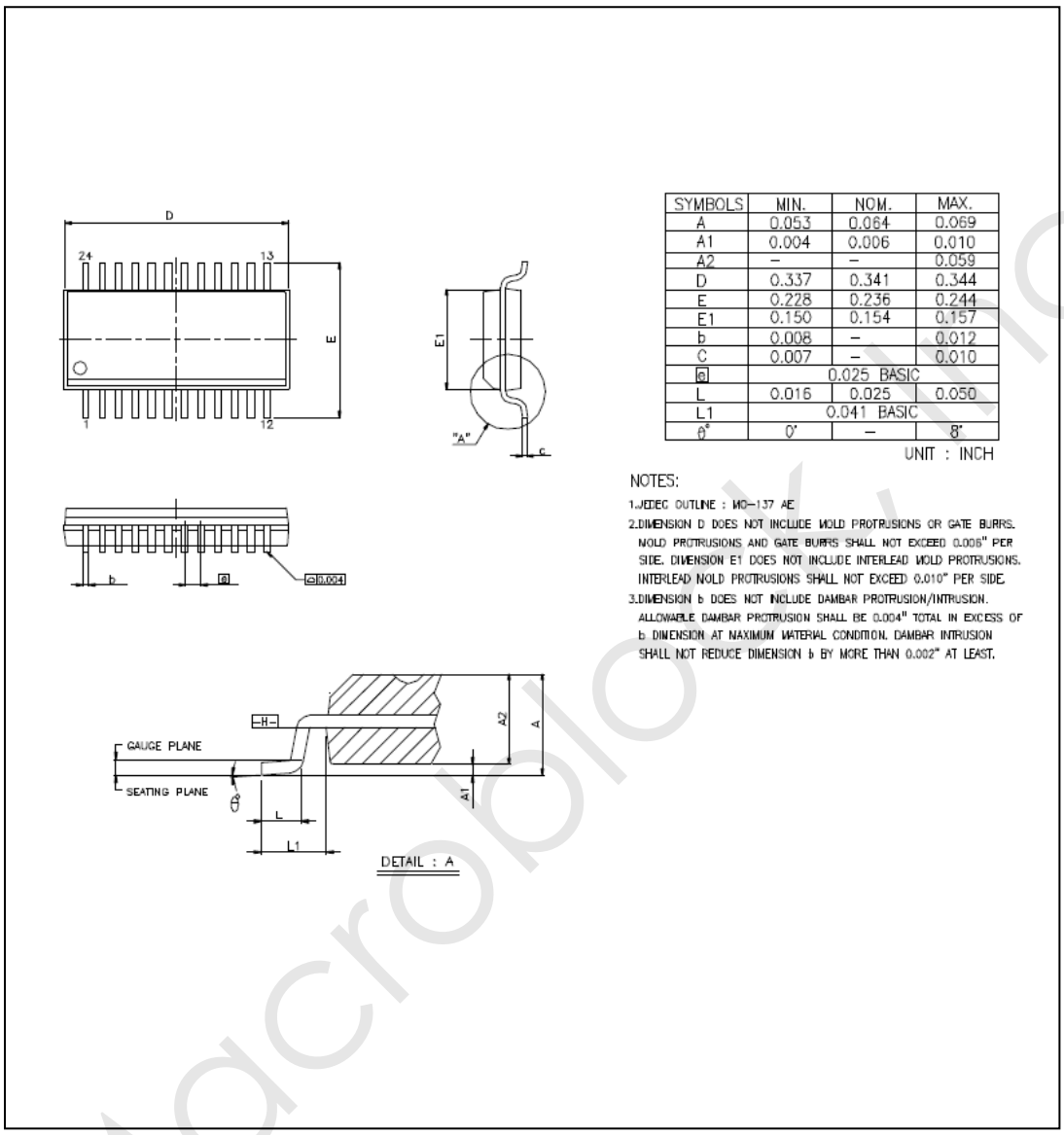
Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245℃ to 260℃ for proper soldering on boards, referring to JEDEC J-STD-020C as shown below. .



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

*Note: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	–	–	0.059
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
b	0.008	–	0.012
C	0.007	–	0.010
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0°	–	8°

UNIT : INCH

NOTES:

1.JEDEC OUTLINE : MO-137 AE

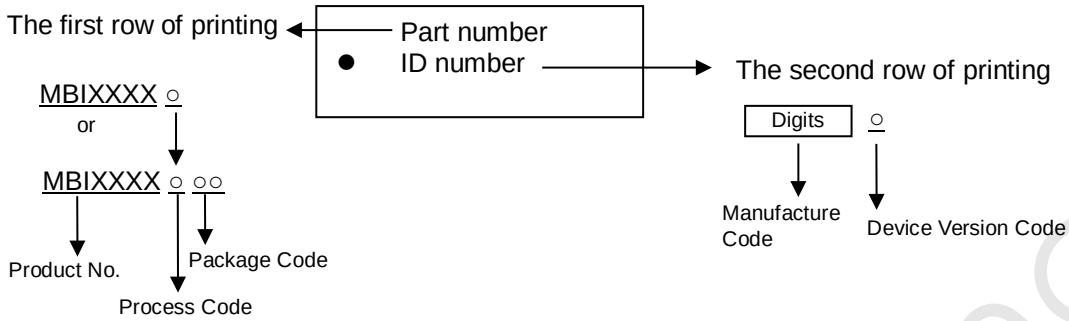
2.DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST.

MBI5262GP Outline Drawing

Note: The unit of the outline drawing is millimeter (mm).

Product Top Mark Information



Product Revision History

Datasheet Version	Device Version Code
V1.00	A

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI5262GP-A	SSOP24L-150-0.64	0.11

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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