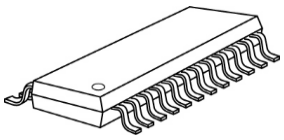
PWM-Embedded 3x4-Channel Constant-Current Sink Driver for LED Strips

Features

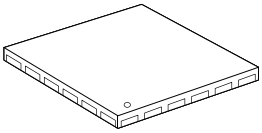
- 3x4-channel constant-current sink driver for LED strips
- Constant current range: 3~45mA
- 3 groups of output current, each group is set by an external resistor
- Sustaining voltage at output channels: 17V (max.)
- Supply voltage 3V~5.5V
- Embedded 16-bit PWM generator
  - Gray scale clock generated by the embedded oscillator
  - S-PWM patented technology
- Two selectable modes to trade off between image quality and transmission bandwidth
  - 16-bit gray scale mode (with optional 8-bit dot correction)
  - 10-bit gray scale mode (with optional 6-bit dot correction)
- Reliable data transmission
  - Daisy-chain topology
  - Two-wire transmission interface
  - Phase-inversed output clock
  - Built-in buffer for long distance transmission
- Flexible PWM reset modes
  - Auto-synchronization mode
  - Manual-synchronization mode
- Selectable polarity reversion to drive high-power drivers or MOSFET
- RoHS-compliant packages
- Package MSL Level : 3

Shrink SOP



GP: SSOP24L-150-0.64

Quad Flat No-Lead



GFN: QFN24L-4*4-0.5

Application

- LED strips
- Mesh display
- Architectural lighting

6F-4, No.18, Pu-Ting Rd., Hsinchu, Taiwan 30072, R.O.C.
TEL: +886-3-579-0068, FAX: +886-3-579-7534, E-mail: info@mblock.com.tw

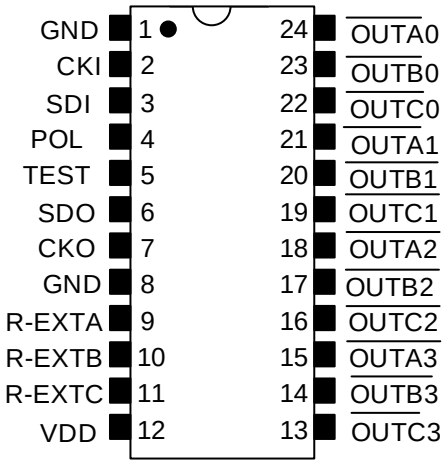
Product Description

MBI6024 is a 3x4-channel, constant-current, PWM-embedded sink driver for LED strips. MBI6024 provides constant current ranging from 3mA to 45mA for each output channel and are adjustable with three corresponding external resistors. Besides, MBI6024 can support both 3.3V and 5V power systems and sustain 17V at output channels.

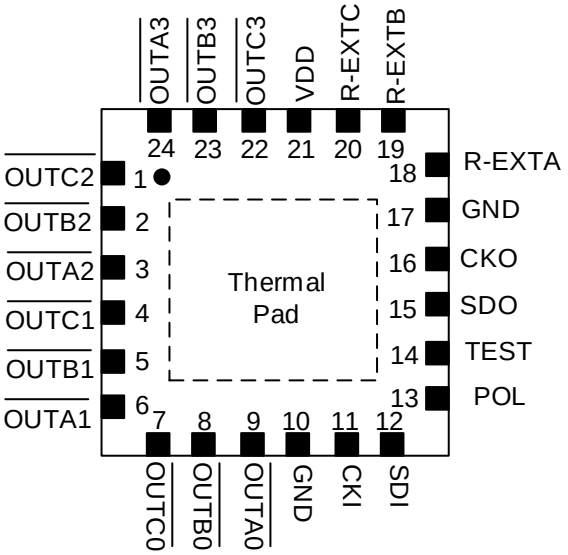
With Scrambled-PWM (S-PWM) technology, MBI6024 enhances pulse width modulation by scrambling the “on” time into several “on” periods to increase visual refresh rate at the same gray scale performance. Besides, the gray scale clock (GCLK) is generated by the embedded oscillator. Moreover, MBI6024 provides two selectable gray scale modes to trade off between image quality and transmission: 16-bit gray scale mode and 10-bit gray scale mode. The 16-bit gray scale mode provides 65,536 gray scales for each LED to enrich the color. Subject to the 16-bit gray scale mode, the 8-bit dot correction may adjust each LED by 256-step gain to compensate the LED brightness. Furthermore, the 10-bit gray scale mode provides 1,024 gray scales. Subject to the 10-bit gray scale mode, 6-bit dot correction may adjust each LED by 64-step gain.

In addition, MBI6024 features a two-wire transmission interface to make cluster-to-cluster connection easier. To improve the transmission quality, MBI6024 provides phase-inversed output clock to eliminate the accumulation of signal pulse width distortion. MBI6024 is also flexible for either manual-synchronization or auto-synchronization. The manual-synchronization is to maintain the synchronization of image frames between ICs. The auto-synchronization is to achieve accurate gray scale, especially when using the built-in oscillator. In addition, MBI6024 preserves selectable polarity reversion to drive high-power drivers or MOSFET as a PWM controller.

Pin Configuration



MBI6024GP
Top View



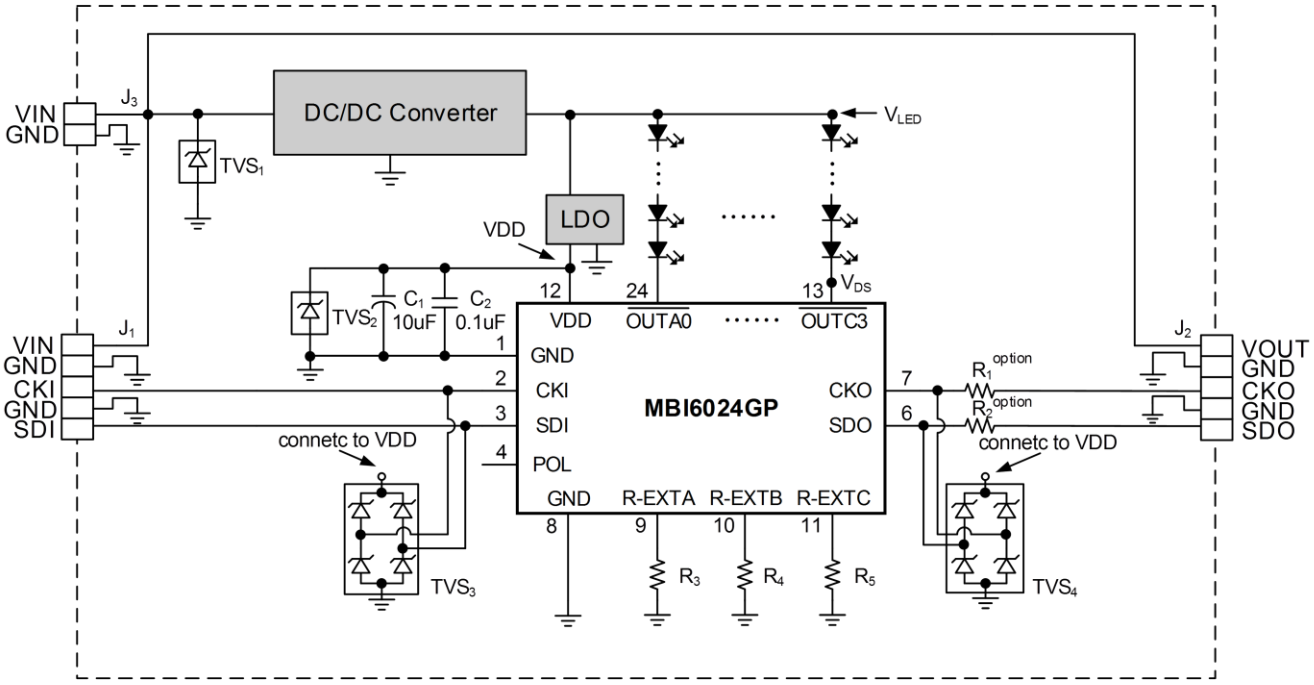
MBI6024GFN
Top View

Terminal Description

Pin		Name	Description and function
GP	GFN		
1	10	GND	Ground terminal
2	11	CKI	Input terminal for clock input
3	12	SDI	Input terminal for serial data input
4	13	POL	Input terminal for selecting output polarity Internal pull-high High: drive LED or low-active regulators or PMOS Low: output reversed to work as a PWM controller to drive high-active regulators or NMOS
5	14	TEST	Test pin (Default: internal pulled- low)
6	15	SDO	Output terminal for serial data output
7	16	CKO	Output terminal for clock output
8	17	GND	Ground terminal
9,10,11	18,19,20	R-EXTA, B, C	Input terminals for setting output current by connecting to an external resistor
12	21	VDD	3.3V/5V supply voltage terminal
15,14,13	24,23,22	$\overline{OUTA3, B3, C3}$	Output terminals for constant-current output
18,17,16	3,2,1	$\overline{OUTA2, B2, C2}$	Output terminals for constant-current output
21,20,19	6,5,4	$\overline{OUTA1, B1, C1}$	Output terminals for constant-current output
24,23,22	9,8,7	$\overline{OUTA0, B0, C0}$	Output terminals for constant-current output
-	-	Thermal Pad	Heat dissipation pad* Please connect to GND.

*The desired thermal conductivity will be improved on condition that a heat-conducting copper foil on PCB is soldered with thermal pad.

Typical Application Circuit



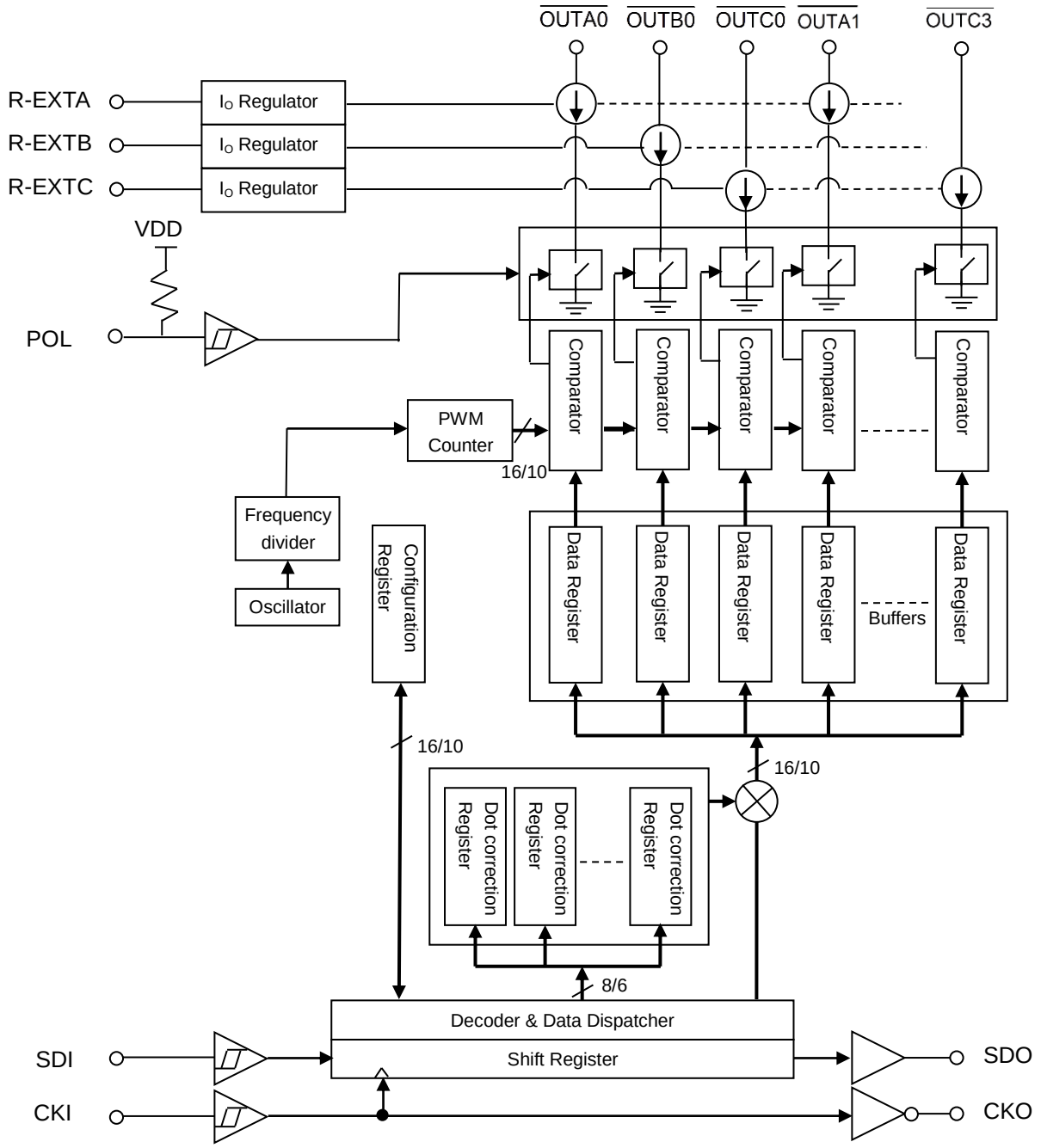
Note:

1. TVS_1~TVS_4 are Transient Voltage Suppressor (TVS).

2. C_1~C_2 are required. The values of the C_1~C_2 are reference only. Tantalum capacitors and Ceramic capacitors are recommended.

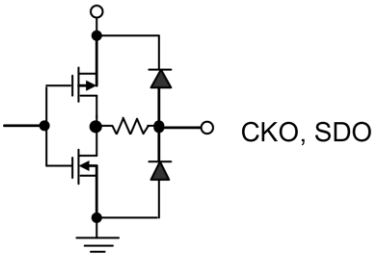
3. For hot plug, system grounding, connector design, external ESD protection, or detailed circuit information, please refer to the ***"MBI6024 Application Note"*** for detailed information.

Block Diagram

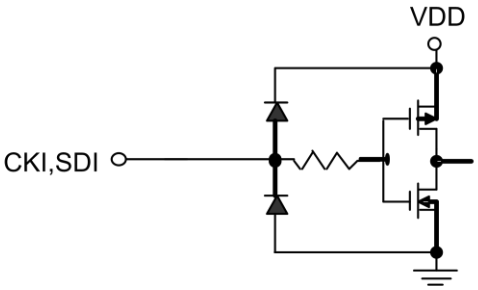


Equivalent Circuits of Inputs and Outputs

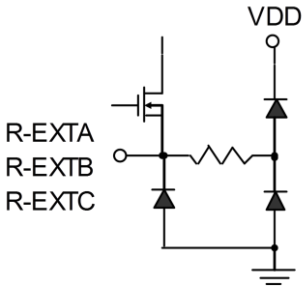
CKO, SDO terminal



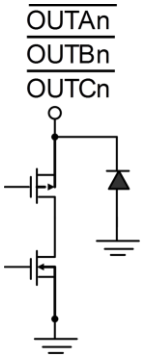
CKI, SDI terminal



R-EXTA, B, C terminal



$\overline{\text{OUTAn,Bn,Cn}}$ terminal



Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Sustaining Voltage at CKI, SDI Pins		V_{IN}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at CKO, SDO Pins		V_{OUT}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at $\overline{OUTn}$ Pins		V_{DS}	-0.5~+17	V
Output Current per Output Channel		I_{OUT}	+45	mA
GND Terminal Current		I_{GND}	570	mA
Heat dissipation (On 4-Layer PCB, Ta=25°C)*	GP	P_D	1.76	W
	GFN	P_D	3.19	W
Thermal Resistance (By simulation, on 4-Layer PCB)*	GP	$R_{th(j-a)}$	70.90	°C/W
	GFN	$R_{th(j-a)}$	39.15	°C/W
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	Human Body Mode (MIL-STD-883H Method 3015.8)	HBM	Class 3A (5KV)	-
	Machine Mode (ANSI/ESD S5.2-2009,)	MM	Class M4 (400V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUTAn}$~$\overline{OUTCn}$=Off		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		5	-	45	mA
Driving Current		I_{OH}	CKO, SDO at V_{OH}=4.8V		1.8	2.2	2.5	mA
		I_{OL}	CKO, SDO at V_{OH}=0.2V		2.0	2.3	2.8	mA
Output Leakage Current		I_{OUT}	V_{DS}=17.0V, $\overline{OUTAn}$~$\overline{OUTCn}$ =Off		-	-	1.0	μA
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=7.3KΩ	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=7.3KΩ	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V,		-	±0.1	±0.5	%/V
Output Current vs. Supply Voltage Regulation*		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V		-	±1.0	±2.0	%/V
Input Voltage of CKI, SDI Pins	"H" level	V_{IH}	-		0.73 x V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	-		GND	-	0.28 x V_{DD}	V
Output Voltage of CKO, SDO Pins	"H" level	V_{OL}	I_{OL}=+3.0mA		-	-	0.2	V
	"L" level	V_{OH}	I_{OH}=-3.0mA		V_{DD}-0.2	-	-	V
Voltage at R-EXTA,B,C Pins		V_{REXT}	$\overline{OUTAn}$~$\overline{OUTCn}$=On		1.1	1.22	1.32	V
Knee Voltage*		V_{Knee}	R_{ext}=3.3KΩ at I_{OUT}=45mA		0.7	0.75	0.8	V
Supply Current**	"Off"	I_{DD}(off)	R_{ext}=4.88KΩ, CKI, SDI=Low, CKO, SDO=NC, $\overline{OUTAn}$~$\overline{OUTCn}$=Off		6.5	7.5	8.5	mA
	"On"	I_{DD}(on)	R_{ext}=7.3KΩ, CKI, SDI=Low, CKO, SDO=NC, $\overline{OUTAn}$~$\overline{OUTCn}$=On		4.8	5.5	6.5	
			R_{ext}=7.3KΩ, CKI=10MHz, CKO, SDO=NC, $\overline{OUTAn}$~$\overline{OUTCn}$=On		-	9	10	

*One channel turns on.

** The supply current may vary with the loading conditions.

Electrical Characteristics (V_{DD}=3.3V, Ta=25˚C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUTAn}$~$\overline{OUTCn}$=Off		-	-	17.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		3	-	30	mA
Driving Current		I_{OH}	CKO, SDO at V_{OH}=3.1V		1.6	1.9	2.4	mA
		I_{OL}	CKO, SDO at V_{OH}=0.2V		1.6	2.1	2.5	mA
Output Leakage Current		I_{OUT}	V_{DS}=17.0V, $\overline{OUTAn}$~$\overline{OUTCn}$ =Off		-	-	1.0	μA
Current Skew (Channel)		dI_{OUT}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=7.3KΩ	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=7.3KΩ	-	±3.0	±6.0	%
Output Current vs. Output Voltage Regulation*		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.5	%/V
Output Current vs. Supply Voltage Regulation*		$\%/dV_{DD}$	V_{DD} within 3.0V and 3.6V		-	±1.0	±2.0	%/V
Input Voltage of CKI, SDI Pins	"H" level	V_{IH}	-		0.73 x V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	-		GND	-	0.28 x V_{DD}	V
Output Voltage of CKO, SDO Pins	"H" level	V_{OL}	I_{OL}=+2.0mA		-	-	0.2	V
	"L" level	V_{OH}	I_{OH}=-2.0mA		V_{DD}-0.2	-	-	V
Voltage at R-EXTA,B,C Pins		V_{REXT}	$\overline{OUTAn}$~$\overline{OUTCn}$=On		1.1	1.22	1.32	V
Knee Voltage*		V_{Knee}	R_{ext}=4.88KΩ at I_{OUT}=30mA		0.80	0.82	0.84	V
Supply Current**	"Off"	I_{DD}(off)	R_{ext}=4.88KΩ, CKI,SDI=Low, CKO, SDO= NC, $\overline{OUTAn}$~ $\overline{OUTCn}$=Off		-	6.5	7.5	mA
	"On"	I_{DD}(on)	R_{ext}=7.3KΩ, CKI,SDI=Low, CKO, SDO=NC, $\overline{OUTAn}$~ $\overline{OUTCn}$=On		-	5.5	6.5	
			R_{ext}=7.3KΩ, CKI=10MHz, CKO, SDO=NC, $\overline{OUTAn}$~ $\overline{OUTCn}$=On		-	6.5	7.5	

*One channel turns on.

**The supply current may vary with the loading conditions.

Switching Characteristics (V_{DD}=5.0V, Ta=25˚C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI–CKI↓	t_{SU}	V_{LED}=4V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND I_{OUT}=20mA R_L=150Ω C_L=10pF C1=4.7uF C2=0.1uF C3=4.7uF C_{CKO}=8pF C_{SDO}=8pF	7.5	-	-	ns
Hold Time	CKI↓–SDI	t_{HD}		7.5	-	-	ns
Propagation Delay Time (“H” to “L”)	CKI↑–CKO↓	t_{PHL1}		-	49		ns
	CKI↓–SDO↑↓	t_{PHL2}		-	44		ns
	GCLK↑– $\overline{OUTB0}$, $\overline{OUTA1}$, $\overline{OUTB2}$ ↓	t_{PHL3}		22	30	38	ns
	GCLK↑– $\overline{OUTC1}$, $\overline{OUTA3}$, $\overline{OUTC3}$ ↓	t_{PHL4}		27	35	43	ns
	GCLK↑– $\overline{OUTA0}$, $\overline{OUTC0}$, $\overline{OUTA2}$ ↓	t_{PHL5}		32	40	48	ns
	GCLK↑– $\overline{OUTB1}$, $\overline{OUTC2}$, $\overline{OUTB3}$ ↓	t_{PHL6}		37	45	53	ns
Propagation Delay Time (“L” to “H”)	GCLK↑– $\overline{OUTB0}$, $\overline{OUTA1}$, $\overline{OUTB2}$ ↑	t_{PLH3}		22	30	38	ns
	GCLK↑– $\overline{OUTC1}$, $\overline{OUTA3}$, $\overline{OUTC3}$ ↑	t_{PLH4}		27	35	43	ns
	GCLK↑– $\overline{OUTA0}$, $\overline{OUTC0}$, $\overline{OUTA2}$ ↑	t_{PLH5}		32	40	48	ns
	GCLK↑– $\overline{OUTB1}$, $\overline{OUTC2}$, $\overline{OUTB3}$ ↑	t_{PLH6}		37	45	53	ns
Pulse Width	CKI*	$t_{W(I)}$		15	-	-	ns
Minimum Pulse Width of PWM	$\overline{OUTAn}$~$\overline{OUTCn}$	t_{WDM}		38	-	-	ns
Rise Time	CKO/SDO	t_{OR}		2.0	3.5	5.0	ns
	$\overline{OUTAn}$~$\overline{OUTCn}$	t_{OR1}		8.0	12.0	15.0	ns
Fall Time	CKO/SDO	t_{OF}		2.0	3.5	5.0	ns
	$\overline{OUTAn}$~$\overline{OUTCn}$	t_{OF1}		12.0	16.0	20.0	ns
Frequency	CKI*	F_{CKI}		0.2	-	10	MHz
	Internal Oscillator	F_{OSC}		24	26	28	MHz

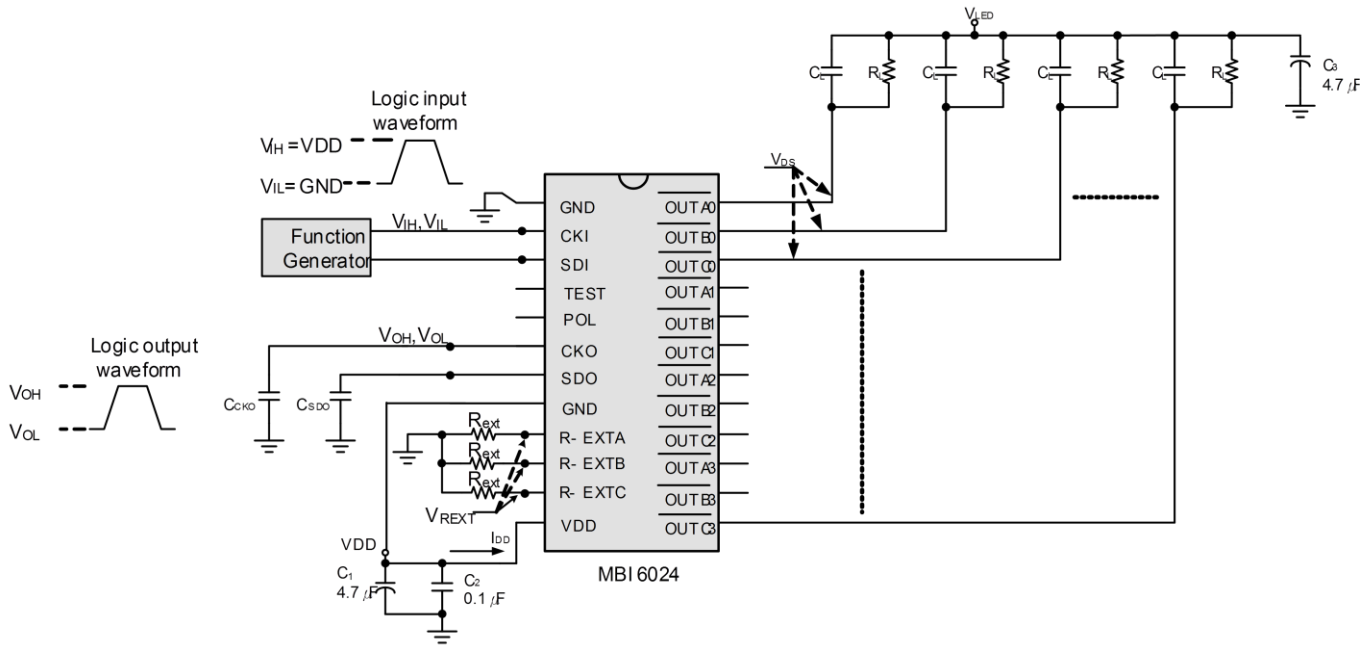
*The maximum frequency may be limited by different application conditions. Please refer to the application note for details.

Switching Characteristics (V_{DD}=3.3V, Ta=25˚C)

Characteristics			Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI–CKI↓		t_{SU}	V_{LED}=4V V_{DS}=1.0V V_{IH}=V_{DD} V_{IL}=GND I_{OUT}=20mA R_L=150Ω C_L=10pF C1=4.7uF C2=0.1uF C3=4.7uF C_{CKO}=8pF C_{SDO}=8pF	7.5	-	-	ns
Hold Time	CKI↓–SDI		t_{HD}		7.5	-	-	ns
Propagation Delay Time (“H” to “L”)	CKI↑–CKO↓		t_{PHL1}		-	75	-	ns
	CKI↓–SDO↑↓		t_{PHL2}		-	67	-	ns
	GCLK↑– $\overline{OUTB0}$, $\overline{OUTA1}$, $\overline{OUTB2}$ ↓		t_{PHL3}		32	40	48	ns
	GCLK↑– $\overline{OUTC1}$, $\overline{OUTA3}$, $\overline{OUTC3}$ ↓		t_{PHL4}		40	48	56	ns
	GCLK↑– $\overline{OUTA0}$, $\overline{OUTC0}$, $\overline{OUTA2}$ ↓		t_{PHL5}		48	56	64	ns
	GCLK↑– $\overline{OUTB1}$, $\overline{OUTC2}$, $\overline{OUTB3}$ ↓		t_{PHL6}		56	64	72	ns
Propagation Delay Time (“L” to “H”)	GCLK↑– $\overline{OUTB0}$, $\overline{OUTA1}$, $\overline{OUTB2}$ ↑		t_{PLH3}		32	40	48	ns
	GCLK↑– $\overline{OUTC1}$, $\overline{OUTA3}$, $\overline{OUTC3}$ ↑		t_{PLH4}		40	48	56	ns
	GCLK↑– $\overline{OUTA0}$, $\overline{OUTC0}$, $\overline{OUTA2}$ ↑		t_{PLH5}		48	56	64	ns
	GCLK↑– $\overline{OUTB1}$, $\overline{OUTC2}$, $\overline{OUTB3}$ ↑		t_{PLH6}		56	64	72	ns
Pulse Width	CKI*		$t_{W(I)}$		20	-	-	ns
Minimum Pulse Width of PWM	$\overline{OUTAn}$~$\overline{OUTCn}$		t_{WDM}		38	-	-	ns
Rise Time	CKO/SDO		t_{OR}		3.0	6.0	9.0	ns
	$\overline{OUTAn}$~$\overline{OUTCn}$		t_{OR1}		12.0	18.0	24.0	ns
Fall Time	CKO/SDO		t_{OF}		3.0	6.0	9.0	ns
	$\overline{OUTAn}$~$\overline{OUTCn}$		t_{OF1}		30.0	35.0	40.0	ns
Frequency		CKI*	F_{CKI}		0.2	-	10	MHz
		Internal Oscillator	F_{OSC}		24	26	28	

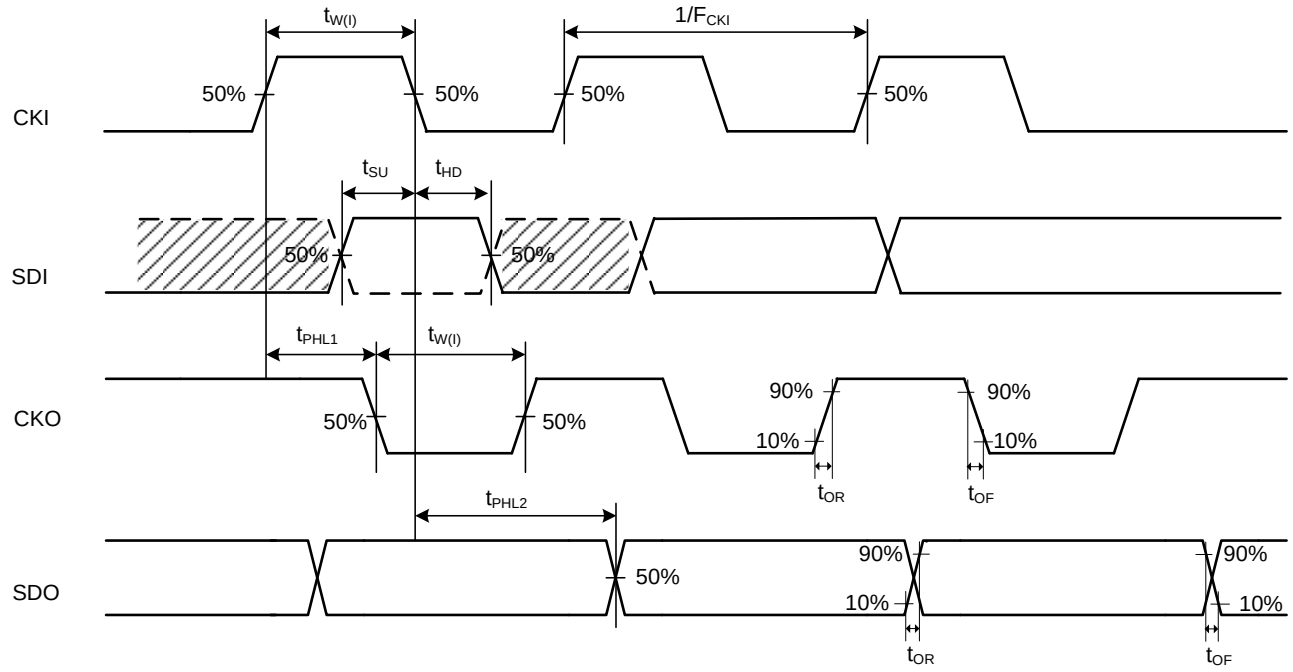
*The maximum frequency may be limited by different application conditions. Please refer to the application note for details.

Test Circuit for Electrical / Switching Characteristics

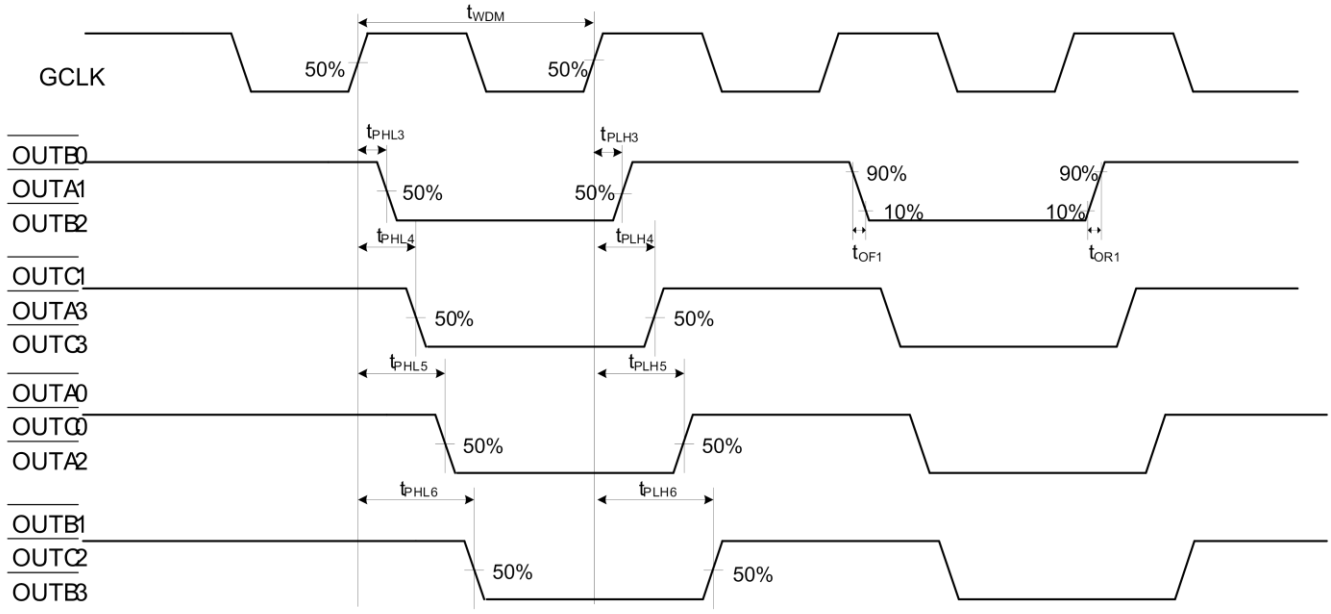


Timing Waveform

Signal Input and Output with Phase-inversed Output Clock



Output Timing



Principle of Operation

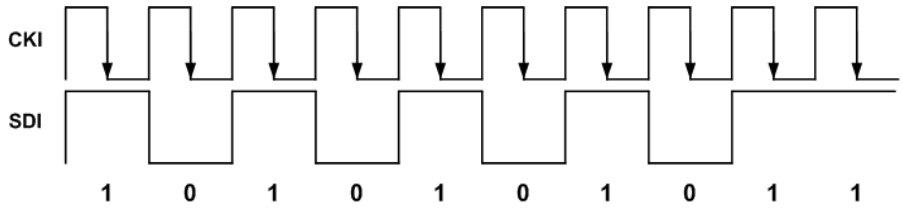
MBI6024 provides SPI-like interface (CKI, SDI), a two-wire transmission interface, to address the data, so that MBI6024 receives the data directly without a latch command. The sequence of operation should follow the steps below:

Step 1. Set the configuration register
Step 2. Send the dot correction data
Step 3. Send the gray scale data

MBI6024 receives the data packet containing targeted gray scale (GS) data from the controller, and turns on the output channels according to the gray scale data. The gray scale clock of PWM generator, GCLK, is generated by the embedded oscillator.

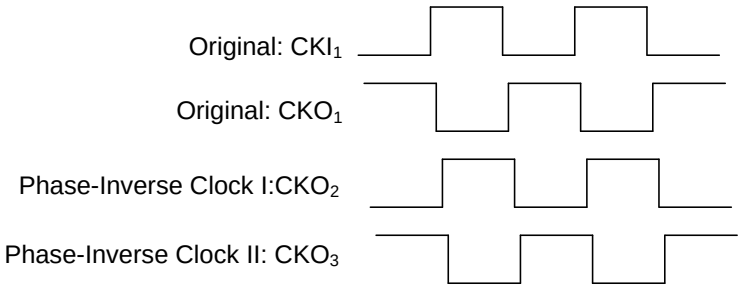
Control Interface: SPI-Like Interface (CKI, SDI)

MBI6024 adopts the SPI-like interface (CKI/SDI). By SPI-like interface, MBI6024 samples the data (SDI) at the falling edge of the clock (CKI).The following waveforms is the example of the SPI-like interface.



Phase-inversed Output Clock

MBI6024 enhances the capability of cascading MBI6024 by phase-inversed output clock function. By phase-inversed output clock, the clock phase will be inversed from CKI to CKO to eliminate the accumulation of the pulse width deviation. This improves the signal integrity of data transmission. The following chart illustrates the phase-inversed output clock results.



The Structure of Data Packet

MBI6024's data packet contains three parts:

1. Prefix:
   The prefix is a symbol of "Silent-to-Reset", i.e. a time period for MBI6024 to distinguish two data packets. During the prefix, both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.
2. Header:
   The header defines the cascaded IC numbers and also contains a command to decide the data type.
3. Data:
   This is the data for each IC. It may be gray scale data, dot correction data, or configuration data.

Structure of a data packet:

Prefix	Header	Data

Setting the Data Types by the Command

MBI6024 provides six kinds of commands and input data types shown as the table below:

Command H[5:0]	**Data Type**
6'b11 1111	16-bit gray scale data
6'b10 1011	10-bit gray scale data
6'b11 0011	8-bit dot correction data
6'b10 0111	6-bit dot correction data
6'b10 0011	16-bit configuration data
6'b11 0111	10-bit configuration data

Once MBI6024 receives the SDI=1 (1'b1), MBI6024 will start to check if the data is a valid command or not. If the 6-bit data is a valid command, the driver will latch the specific data according to the protocol. If the 6-bit data is not a valid command, MBI6024 will wait for another SDI=1 (1'b1) to check the validity of the next command.

When enable function of polarity reversion, by connecting pin POL to GND, MBI6024 would only accept 10-bit grayscale command listed below

Command H[5:0]	**Data Type**
6'b10 1011	10-bit gray scale data

Time-Out Reset for Transmission Abort

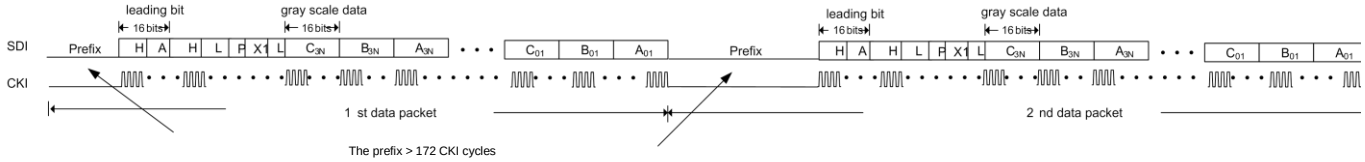
Time-out reset is to prevent ICs from misreading during the data transmission. If the CKI is tied-low for more than 2 CKI cycles, MBI6024 may identify the wires as disconnection. To prevent from misreading, MBI6024 will ignore the present input data and continuously show the previous image data until the next image data is correctly recognized.

The Prefix in the Beginning of a Data Packet

MBI6024 identifies the data as a new data packet after time-out, so the prefix in the beginning of a data packet should be more than 172 CKI cycles.

If both CKI and SDI are tied-low and stop for more than the setting of CKI time-out period, MBI6024 will start to check the valid command of the next data packet. The prefix between two data packets helps MBI6024 identify the

data packet correctly. The following timing diagram illustrates the interval between two data packets in 16-bit gray scale mode.



Definition of Configuration Register

MBI6024 provides two configuration register sections: configuration register 1 (CF1) and configuration register 2 (CF2) as defined in the tables below.

Configuration Register 1 (CF1):

	MSB									LSB
Bit	9	8	7	6	5	4	3	2	1	0
Default Value	10		0	11		1	1	11		0

Note: Bit [15:10] should be set as “0” to avoid signal misjudgment.

Bit	Definition	Value	Function
9:8	GCLK frequency	11	GCLK=frequency of internal oscillator, i.e. 24MHz (typical).
		10 (default)	GCLK=oscillator frequency divided by two, i.e. 12MHz (typical).
		01	GCLK=oscillator frequency divided by four, i.e. 6MHz (typical).
		00	GCLK= oscillator frequency divided by eight, i.e. 3MHz (typical).
7	Dot correction mode	0 (default)	enable dot correction,
		1	bypass dot correction
6:5	Reserved	11 (default)	Must fill in ‘11’
4	PWM counter reset	1 (default)	Reset PWM counter after programming configuration register
		0	Do not reset PWM counter after programming configuration register
3	PWM data synchronization	1 (default)	Automatic synchronization
		0	Manual synchronization
2:1	Phase-inversed output clock	11 (default)	The waveform is inversed from CKI to CKO; please set the two bits as 2b’11. Other combinations are reserved for internal tests.
0	Parity check	1	Enable
		0 (default)	Disable

GCLK Frequency

MBI6024 provides four kinds of internal GCLK frequency, which is the internal oscillator frequency divided by 1, 2, 4, and 8, for different applications according to the bits of CF1[9:8]. The internal oscillator frequency is 24MHz (typ.); e.g. if the internal oscillator frequency is divided by 8, the GCLK frequency is 3MHz.

Higher GCLK frequency provides higher visual refresh rate, but also higher EMI. If the output current is larger than 40mA, the GCLK frequency is suggested to be lower than 8MHz to keep good linearity at low gray scale level.

Dot Correction Mode

MBI6024 also provides 8-bit or 6-bit dot correction in 16-bit or 10-bit gray scale mode respectively. Dot correction control helps compensate LED brightness and reduces the loading of calculation in controllers. In addition, with the built-in multiplier, MBI6024 operates dot correction without sacrificing the visual refresh rate.

PWM Counter Reset

MBI6024 can optionally reset the PWM counter by setting the bit of CF1[4] after programming configuration register. The default setting is to reset the PWM counter to start a new PWM cycle to align the PWM output data for new setting.

PWM Data Synchronization

MBI6024 is also flexible for either manual-synchronization or auto-synchronization by setting the bit of CF1[3]. For auto-synchronization, the bit of CF1[3] is set to “1” (default). MBI6024 will automatically process the synchronization of previous data and next data for PWM counting. The next image data will be updated to output buffers and start PWM counting when the previous data finishes one internal PWM cycle.

For manual-synchronization, the bit of CF1[3] is set to “0”. Once the next input data is correctly recognized, MBI6024 will stop the present PWM cycle and restart a new PWM cycle to show the new data immediately.

The advantage of manual-synchronization is to maintain the synchronization of image frames between ICs, but the PWM cycle may not be finished, so the gray scale accuracy is slightly affected. Since S-PWM scrambles the 16-bit PWM cycle into 64 small periods, the gray scale accuracy remains good. For better gray scale performance, auto-synchronization keeps accurate gray scale especially when using the built-in oscillator, but the drawback is the synchronization of image frames between ICs.

Parity Check

Parity check is to check the data in the header for any error, especially to prevent the configuration register and dot correction register from miswriting.

Configuration Register 2 (CF2):

Default Value

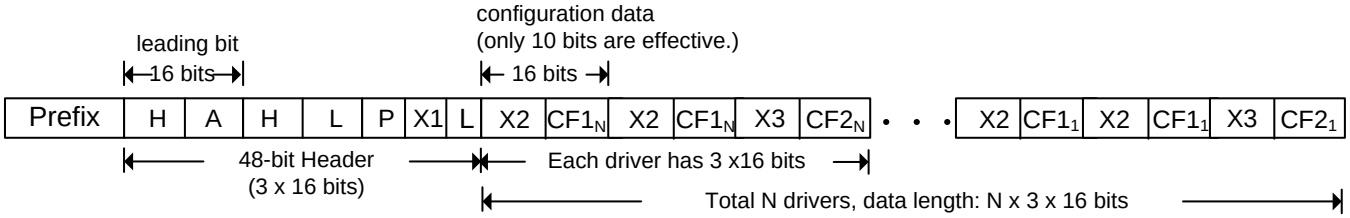
	MSB		LSB
Bit	2	1	0
Value	111		

Note: Bit [15:3] should be set as “0” to avoid signal misjudgment.

Bit	Definition	Value	Function
2	Reserved	1 (default)	Must fill in ‘1’
1:0	Reserved	11 (default)	Must fill in ‘11’

16-bit Configuration Data

For 16-bit configuration data, each word is 16 bits. Each MBI6024 needs 3 words (3x16=48 bits) for the configuration data. However, each configuration data has only 10 bits, and the MSB 6 bits of each word are invalid. Prior to the configuration data, there is a 48-bit header. MBI6024 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

48-bits header

Bit	Definition	Value	Function
47:42	H[5:0]	100011	The command of 16-bit configuration data
41:32	A[9:0]	0000000000	Address data. Always send 10’b 0000000000
31:26	H[5:0]	100011	Double check the command. It should be the same as the prior H[5:0], otherwise the data packet will be ignored.
25:16	L[9:0]	N-1 N=Number of IC in series	Set the number of IC in series
15:12	P[3:0]	0000~1111	P[3:0] are parity check bits, If it is incorrect, the data packet will be ignored. P[0] is the parity check bit of L[9:0] P[0]=1 if the count of “1” within L[9:0] is odd; P[0]=0 if the count of “1” within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of “1” within A[9:0] is odd; P[1]=0 if the count of “1” within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of “1” within H[5:0] is odd; P[2]=0 if the count of “1” within H[5:0] is even.

			P[3] is the parity check bit of P[2:0] P[3]=1 if the count of “1” within P[2:0] is odd; P[3]=0 if the count of “1” within P[2:0] is even.
11:10	X1[1:0]	XX	Don’t care. The value is suggested to be “0”.
9:0	L[9:0]	N-1 N=Number of IC in series	Double check the number of IC in series

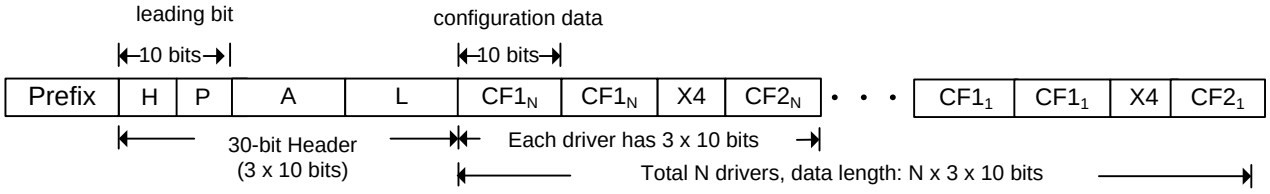
48-bit configuration data

Bit	Definition	Value	Function
47:0	X2[5:0]~$CF1_N$[9:0]~ X2[5:0]~$CF1_N$[9:0]~ X3[12:0]~$CF2_N$[2:0]	48b’0~48b’1	X2[5:0] are “don’t care” bits. The value is suggested to be “0”. $CF1_N$[9:0] are 10 bits data of configuration register 1 (CF1). The 2^{nd} CF1[9:0] double checks the data of configuration register bank 1 (CF1). It should be the same as the 1^{st} $CF1_N$[9:0]; otherwise the data will not be written into register. X3[12:0] are “don’t care” bits. The value is suggested to be “0”. $CF2_N$[2:0] are 3 bits data of configuration register 2 (CF2)

The configuration data of the last IC is sent first, followed by the previous ICs, and the first IC’s configuration data is sent in the end of the packet.

10-bit Configuration Data

For 10-bit configuration data, each word is 10 bits. Each MBI6024 needs 3 words (3x10=30 bits) for the configuration data. Prior to the configuration data, there is a 30-bit header. MBI6024 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

30-bit header

Bit	Definition	Value	Function
29:24	H[5:0]	110111	The command of 10-bit configuration data
23:20	P[3:0]	0000~1111	P[3:0] are parity check bits, If it is incorrect, the data packet will be ignored. P[0] is the parity check bit of L[9:0]. P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
19:10	A[9:0]	0000000000	Address data. Always send 10'b 0000000000
9:0	L[9:0]	N-1 N=Number of IC in series	Set the number of IC in series

30-bit configuration data

Bit	Definition	Value	Function
29:0	$CF1_N$[9:0]~$CF1_N$[9:0]~X4[6:0]~$CF2_N$[2:0]	30b'0~30b'1	CF1[9:0] are 10 bits data of configuration register 1 (CF1). The 2nd CF1[9:0] double checks the data of configuration register 1 (CF1). It should be the same as the 1st CF1[9:0]; otherwise the data will not be written into register. X4[6:0] are "don't care" bits. The value is suggested to be "0". CF2[2:0] are 3 bits data of configuration register 2 (CF2)

The configuration data of the last IC is sent first, followed by the previous ICs, and the first IC's configuration data is sent in the end of the packet.

Gray Scale

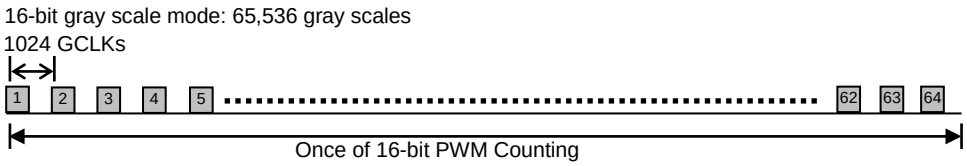
MBI6024 provides two gray scale modes: 16-bit gray scale mode and 10-bit gray scale mode by adopting S-PWM or conventional PWM algorithm respectively. MBI6024 adopts S-PWM technology in 16-bit gray scale mode to scramble the 16-bit PWM to 64 segments, so that the visual refresh rate can be increased. For example, with S-PWM, the default PWM clock (GCLK) frequency is around 12MHz (the frequency of internal oscillator divided by two), and therefore, the visual refresh rate of 16-bit gray scale mode will be increased to: 12MHz/65536x64=11,718Hz

On the other hand, MBI6024 provides 10-bit gray scale mode by conventional PWM. In 16-bit gray scale mode, MBI6024 achieves 65,536 gray scales for each LED, and in 10-bit gray scale mode, MBI6024 achieves 1,024 gray scales. The following illustrations explain the PWM counting by S-PWM and conventional PWM algorithms.

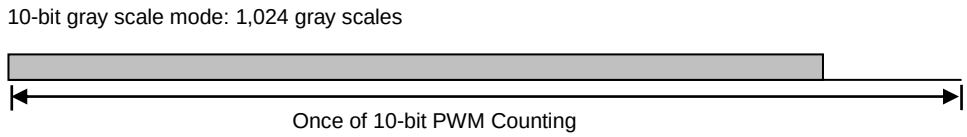
PWM counting by S-PWM or conventional PWM algorithm

With S-PWM technology, the total PWM cycles can be broken down into 64 segments.

16-bit Gray Scale Mode with S-PWM



10-bit Gray Scale Mode with Conventional PWM



Example of 16-bit Gray Scale Data:

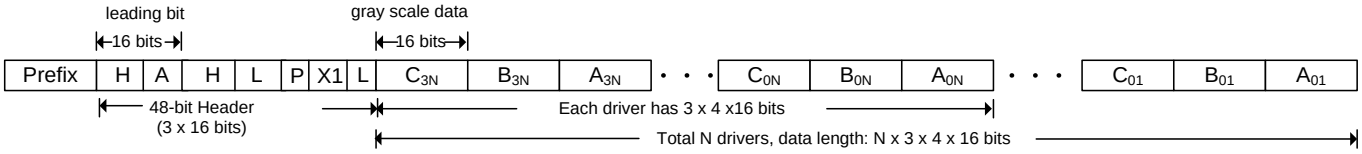
Gray scale data	The ratio of output turn-on time in a PWM cycle
0	$0/2^{16}$
1	$1/2^{16}$
2	$2/2^{16}$
. . .	. . .
65535	$65535/2^{16}$

Example of 10-bit Gray Scale Data:

Gray scale data	The ratio of output turn-on time in a PWM cycle
0	$0/2^{10}$
1	$1/2^{10}$
2	$2/2^{10}$
. . .	. . .
1023	$1023/2^{10}$

16-bit Gray Scale Data

For 16-bit gray scale data, each word is 16 bits. Each MBI6024 needs 12 words (12x16=192 bits) for the gray scale data of each output channel of one MBI6024. Prior to the gray scale data, there is a 48-bit header. MBI6024 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

48-bit header

Bit	Definition	Value	Function
47:42	H[5:0]	111111	The command of 16-bit gray scale data
41:32	A[9:0]	0000000000	Address data. Always send 10'b 0000000000
31:26	H[5:0]	111111	Double check the command. It should be the same as the prior H[5:0], otherwise the data packet will be ignored.
25:16	L[9:0]	N -1 N=Number of IC in series	Set the number of IC in series
15:12	P[3:0]	0000~1111	P[3:0] are parity check bits, If it is incorrect, the data packet will be ignored. P[0] is the parity check bit of L[9:0] P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
11:10	X1[1:0]	XX	Don't care. The value is suggested to be "0".
9:0	L[9:0]	N-1 N=Number of IC in series	Double check the number of IC in series

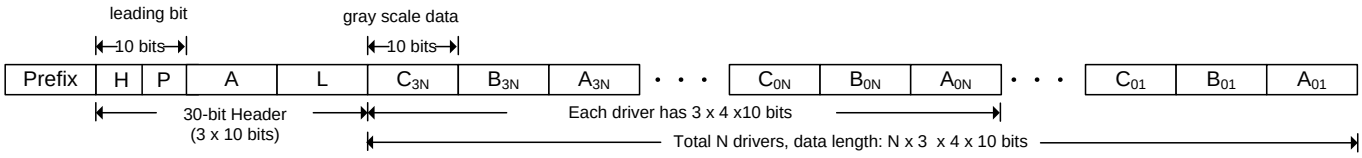
192-bit gray scale data

Bit	Definition	Value	Function
191:0	C_{3N}[15:0]~A_{0N}[15:0]	192b'0~192b'1	16-bit x 12 channels gray scale data of the Nth MBI6024. The data of $\overline{OUTC_{3N}}$ is sent first.

The gray scale data of the last IC is sent first, followed by the previous ICs, and the first IC's gray scale data is sent in the end of the packet.

10-bit Gray Scale Data

For 10-bit gray scale data, each word is 10 bits. Each MBI6024 needs 12 words (12x10=120 bits) for the gray scale data of each output channel of one MBI6024. Prior to the gray scale data, there is a 30-bit header. MBI6024 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

30-bit header

Bit	Definition	Value	Function
29:24	H[5:0]	101011	The command of 10-bit gray scale data
23:20	P[3:0]	0000~1111	P[3:0] are parity check bits, If it is incorrect, the data packet will be ignored. P[0] is the parity check bit of L[9:0]. P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
19:10	A[9:0]	0000000000	Address data. Always send 10'b 0000000000
9:0	L[9:0]	N-1 N=Number of IC in series	Set the number of IC in series

120-bit gray scale data

Bit	Definition	Value	Function
119:0	C_{3N}[9:0]~A_{0N}[9:0]	120b'0~120b'1	10-bit x 12 channels gray scale data of the Nth MBI6024. The data of $\overline{OUTC_{3N}}$ is sent first.

The gray scale data of the last IC is sent first, followed by the previous ICs, and the first IC's gray scale data is sent in the end of the packet.

Polarity reversion

Connecting pin "POL" to GND will enable function of polarity reversion. It will set frequency of internal oscillator to 1.5Mhz and PWM counter to 10-bit mode. Please find more information about it from application note of MBI6024.

Dot Correction

For valid dot correction control, users have to program dot correction data before sending gray scale data.

16-bit gray scale data with 8-bit dot correction

MBI6024 multiplies the 16-bit gray scale data and 8-bit dot correction data internally and truncates the product to 16 bits, so the PWM cycle time remains 65,536 GCLKs.

The following is the equation for the duty cycle of output in 16-bit gray scale mode. For 8-bit dot correction, the default value of dot correction data is 255.

$$\text{The duty cycle of output (\%)} = \frac{\text{16-bit gray scale data} \times \frac{(\text{8-bit dot correction data} + 1)}{256}}{65{,}536} \times 100\%$$

According to the above equation, the following table shows the examples:

Example:

Dot correction data	The ratio of output turn-on time
0	1/256 x gray scale data
1	2/256 x gray scale data
2	3/256 x gray scale data
⋮	⋮
255	256/256 x gray scale data

10-bit gray scale with 6-bit dot correction:

The following is the equation for the duty cycle of output in 10-bit gray scale mode. For 6-bit dot correction, the default value of dot correction data is 63.

$$\text{The duty cycle of output (\%)} = \frac{\text{10-bit gray scale data} \times \frac{(\text{6-bit dot correction data} + 1)}{64}}{1{,}024} \times 100\%$$

According to the above equation, the following table shows the examples:

Example:

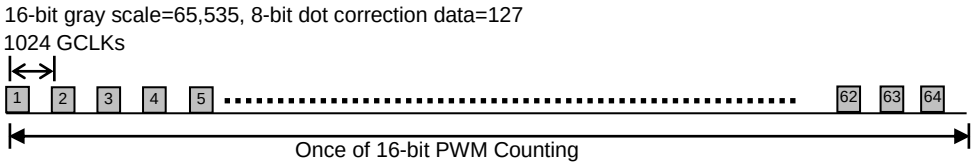
Dot correction data	The ratio of output turn-on time
0	1/64 x gray scale data
1	2/64 x gray scale data
2	3/64 x gray scale data
⋮	⋮
63	64/64 x gray scale data

The algorithm of PWM counting with dot correction data

When adopting 8-bit dot correction in 16-bit gray scale mode, MBI6024 multiplies the 16-bit gray scale data and the 10-bit dot correction data and truncates the product to 16 bits, then uses the corrected 16-bit data to generate PWM output by S-PWM technology. The built-in multiplier facilitates to keep high visual refresh rate.

The chart below illustrates the effect of the built-in multiplier and S-PWM.
Assume:
the 16-bit gray scale data=65,535,
8-bit dot correction data=127 (50%),
then the 16-bit PWM output period is scrambled into 64 segments,
each segment has ~50% duty ratio.

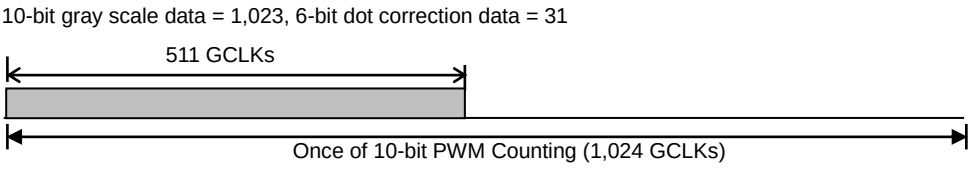
16-bit Gray Scale Data with 8-bit Dot Correction Data



When adopting 6-bit dot correction in 10-bit gray scale mode, MBI6024 multiplies the 10-bit gray scale data and the 6-bit dot correction data and truncates the product to 10 bits, then uses the corrected 10-bit data to generate PWM output by S-PWM technology. The built-in multiplier facilitates to keep high visual refresh rate.

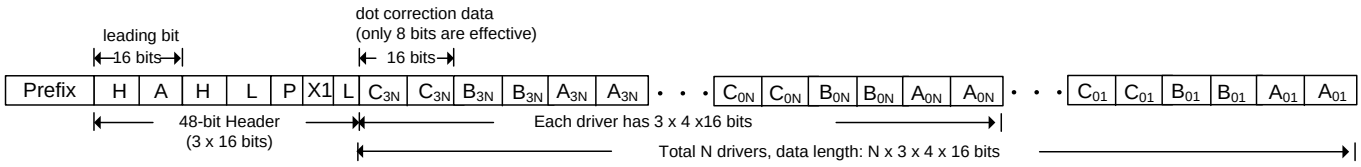
The chart below shows the PWM output.
Assume:
the 10-bit grayscale data=1023,
6-bit dot correction data=31 (50%).
the output duty ratio=511/1024(~50%)。
the output duty cycle=1024 GCLKs。

10 Gray Scale Data with 6-bit Dot Correction Data



8-bit Dot Correction Data

For 8-bit dot correction data, each word is 16 bits. Each MBI6024 needs 12 words (12x16=192 bits) for the dot correction data of each output channel of one MBI6024. However, each dot correction data has only 8 bits, and the first 8 bits of each word are checking bits of dot correction. Prior to the dot correction data, there is a 48-bit header. MBI6024 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

48-bit header

Bit	Definition	Value	Function
47:42	H[5:0]	110011	The command of 8-bit dot correction data
41:32	A[9:0]	0000000000	Address data. Always send 10'b 0000000000
31:26	H[5:0]	110011	Double check the command. It should be the same as the prior H[5:0], otherwise the data packet will be ignored.
25:16	L[9:0]	N-1 N=Number of IC in series	Set the number of IC in series
15:12	P[3:0]	0000~1111	P[3:0] are parity check bits, If it is incorrect, the data packet will be ignored. P[0] is the parity check bit of L[9:0]. P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
11:10	X1[1:0]	XX	Don't care. The value is suggested to be "0".
9:0	L[9:0]	N-1 N=Number of IC in series	Double check the number of IC in series

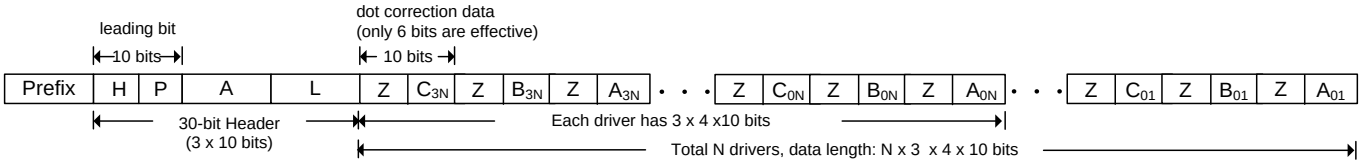
192-bit dot correction data

Bit	Definition	Value	Function
191:0	$C_{3N}[7:0]$~$A_{0N}[7:0]$	192b'0~192b'1	8-bit x 2 x 12 channels dot correction data of the Nth MBI6024. The data of $\overline{OUTC_{3N}}$ is sent first. Sending dot correction data twice is to double check the dot correction data. The two data should be the same; otherwise, the dot correction data of the IC will not be latched.

The dot correction data of the last IC is sent first, followed by the previous ICs, and the first IC's dot correction data is sent in the end of the packet.

6-bit Dot Correction Data

For 6-bit dot correction data, each word is 10 bits. Each MBI6024 needs 12 words (12x10=120 bits) for the dot correction data of each output channel of one MBI6024. However, each dot correction data has only 6 bits, and the first 4 bits of each word should be set as "0". Prior to the dot correction data, there is a 30-bit header. MBI6024 provides parity check function to check the count of bit to prevent the data transmission error. The data format is shown below:



Prefix

Both CKI and SDI should be tied-low and stop for more than 172 CKI cycles.

30-bits header

Bit	Definition	Value	Function
29:24	H[5:0]	100111	The command of 6-bit dot correction data
23:20	P[3:0]	0000~1111	P[3:0] are parity check bits, If it is incorrect, the data packet will be ignored. P[0] is the parity check bit of L[9:0]. P[0]=1 if the count of "1" within L[9:0] is odd; P[0]=0 if the count of "1" within L[9:0] is even. P[1] is the parity check bit of A[9:0] P[1]=1 if the count of "1" within A[9:0] is odd; P[1]=0 if the count of "1" within A[9:0] is even. P[2] is the parity check bit of H[5:0] P[2]=1 if the count of "1" within H[5:0] is odd; P[2]=0 if the count of "1" within H[5:0] is even. P[3] is the parity check bit of P[2:0] P[3]=1 if the count of "1" within P[2:0] is odd; P[3]=0 if the count of "1" within P[2:0] is even.
19:10	A[9:0]	0000000000	Address data. Always send 10'b 0000000000
9:0	L[9:0]	N-1 N=Number of IC in series	Set the number of IC in series

120-bit dot correction data

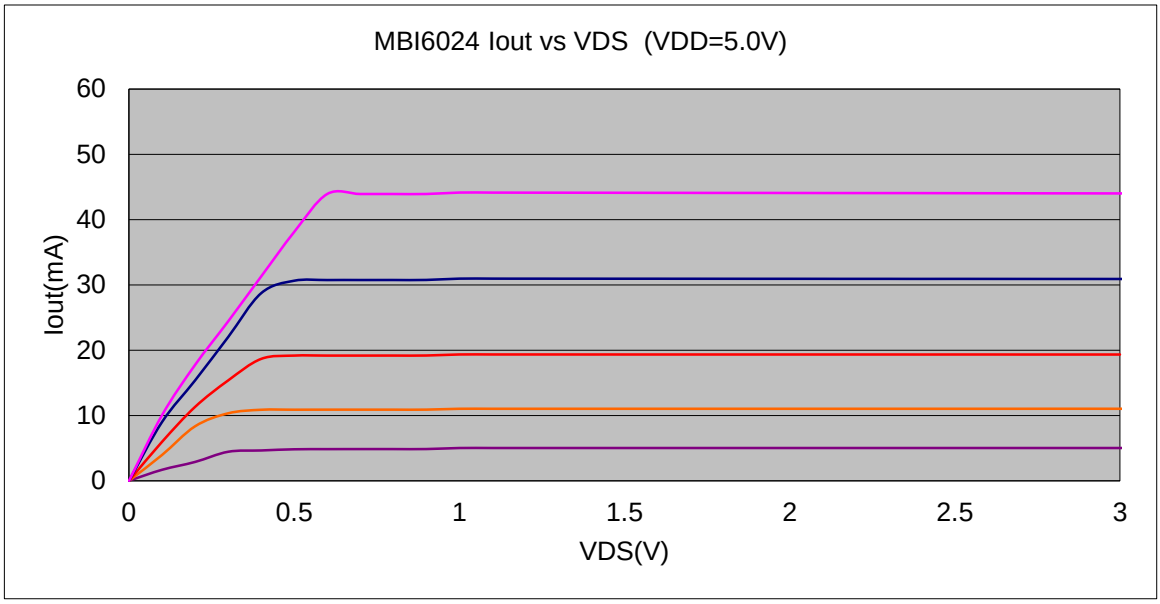
Bit	Definition	Value	Function
119:110	Z[3:0]~C_{3N}[5:0]	10b'0000000000~ 10b'0000111111	(6-bit + 4-bit) x 1 channel dot correction data of the Nth MBI6024. The data of $\overline{OUTC3}$ is sent first. Z[3:0] are check bits. Please send 4b'0000; otherwise, the dot correction data the the IC will not be latched.
109:0	Z[3:0]~B_{3N}[5:0]...A_{0N}[5:0]	The range of the data value is the same as the previous 10 bits.	(6-bit + 4-bit) x 11 channels dot correction data of the Nth MBI6024. The data format is the same as the prior 10 bits.

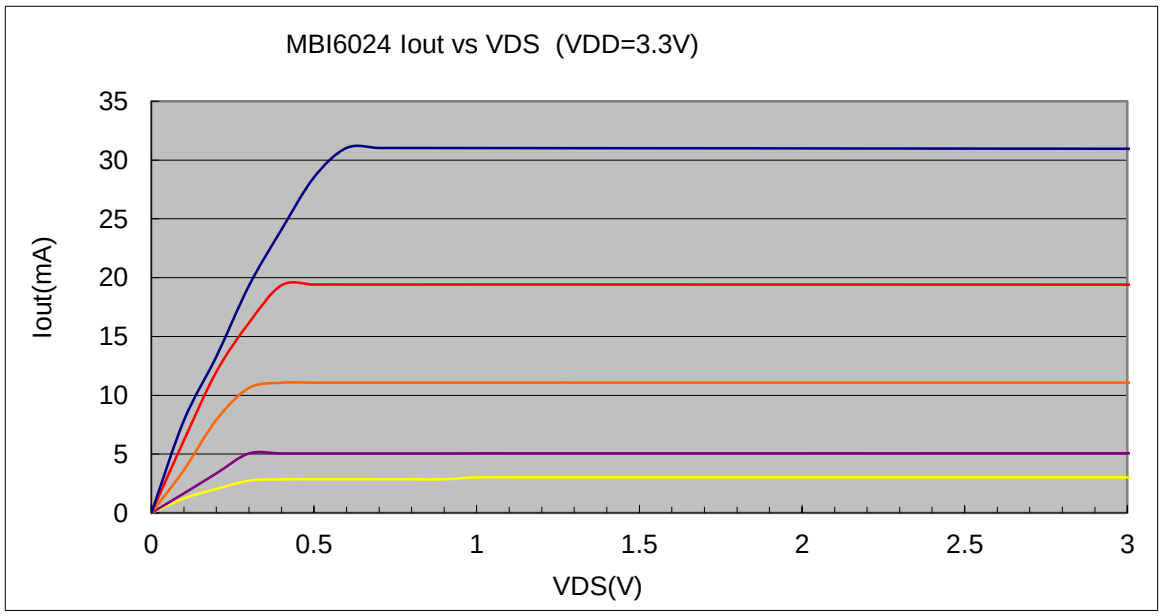
The dot correction data of the last IC is sent first, followed by the previous ICs, and the first IC's dot correction data is sent in the end of the packet. The ratio of output turn-on time will be (dot correction data+1)/256 x gray scale data.

Constant Current

1) MBI6024 performs excellent current skew: the maximum current variation between channels is less than ±3%, and that between ICs is less than ±6%.

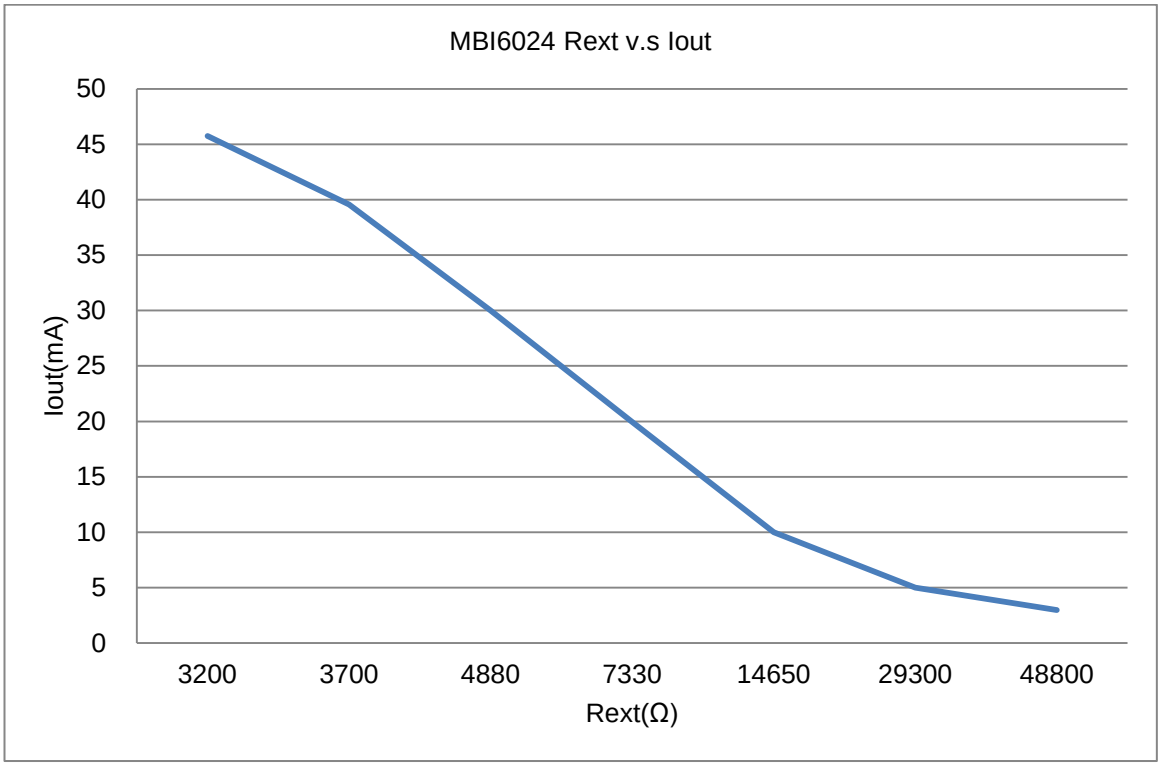
2) In addition, in the saturation region, the output current keeps constant when the output voltage (V_{DS}) is changed. This characteristic guarantees the LED show the same brightness regardless of the variations of LED forward voltages (V_F).





Setting the Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.



The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. When output channels are turned on, V_{REXT} is around 1.22V. The relationship between I_{OUT} and R_{ext} is shown in the following figure.

Also, the output current can be calculated from the equation:

$I_{OUTA}=(V_{REXT}/R_{extA})x120$

$I_{OUTB}=(V_{REXT}/R_{extB})x120$

$I_{OUTC}=(V_{REXT}/R_{extC})x120$

Where R_{extA}, R_{extB}, and R_{extC} are the resistances of the external resistors connected to R-EXTA, R-EXTB, R-EXTC terminals.

Package Heat Dissipation (P_D)

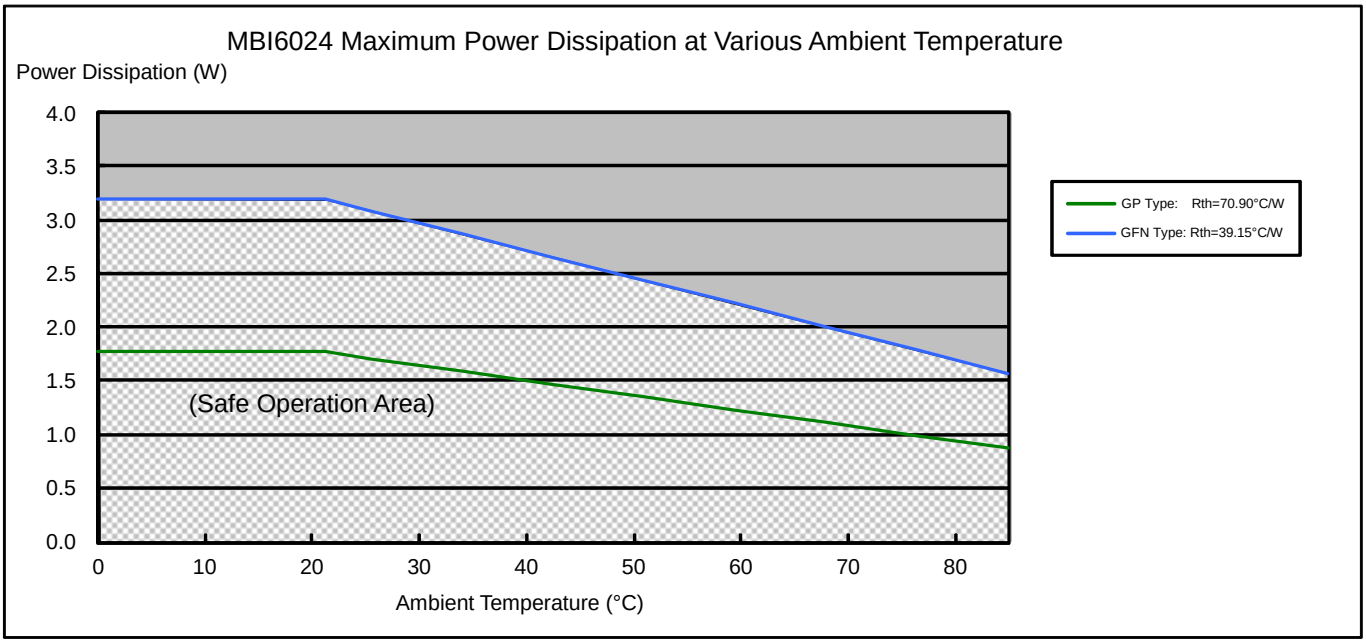
The maximum heat dissipation, $P_{D(max)}=(T_{j,max}–T_a)/R_{th(j-a)}$, decreases as the ambient temperature increases.

The heat dissipation (P_D) of MBI6024 is calculated by the equation:

$$P_D=(V_{DD} \times I_{DD}) + \sum_{i=0}^{i=3} (I_{OUTAi} \times V_{DSAi} \times Duty_{Ai} + I_{OUTBi} \times V_{DSBi} \times Duty_{Bi} + I_{OUTCi} \times V_{DSCi} \times Duty_{Ci})$$

For the calculation of duty cycles, please refer to the “Gray Scale” section.

Please refer to the following figure to design within the safe operation area.



Load Supply Voltage (V_{LED})

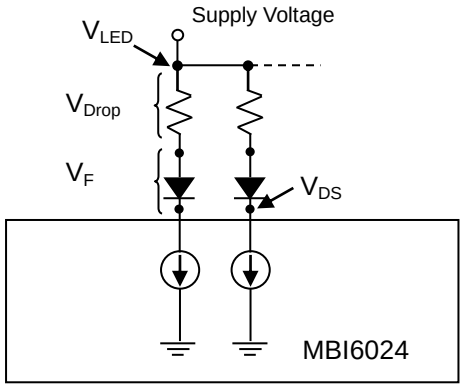
The design of V_{LED} should fulfill two targets:

1. Less power consumption and heat
2. Sufficiently headroom for the LED and driver IC to operate in the constant-current region.

From the figure below, $V_{DS}=V_{LED}–V_F$, which V_{LED} is the supply voltage of LED. $P_{D\ (act)}$ will be greater than $P_{D\ (max)}$, if V_{DS} drops too much voltage on the driver. In this case, it is recommended to use the lowest possible supply voltage or to set an external resistor to reduce the by V_{DROP}.

$V_{DS}=(V_{LED}–V_F)–V_{DROP}$

Please refer to the following figure for the application of the resister.



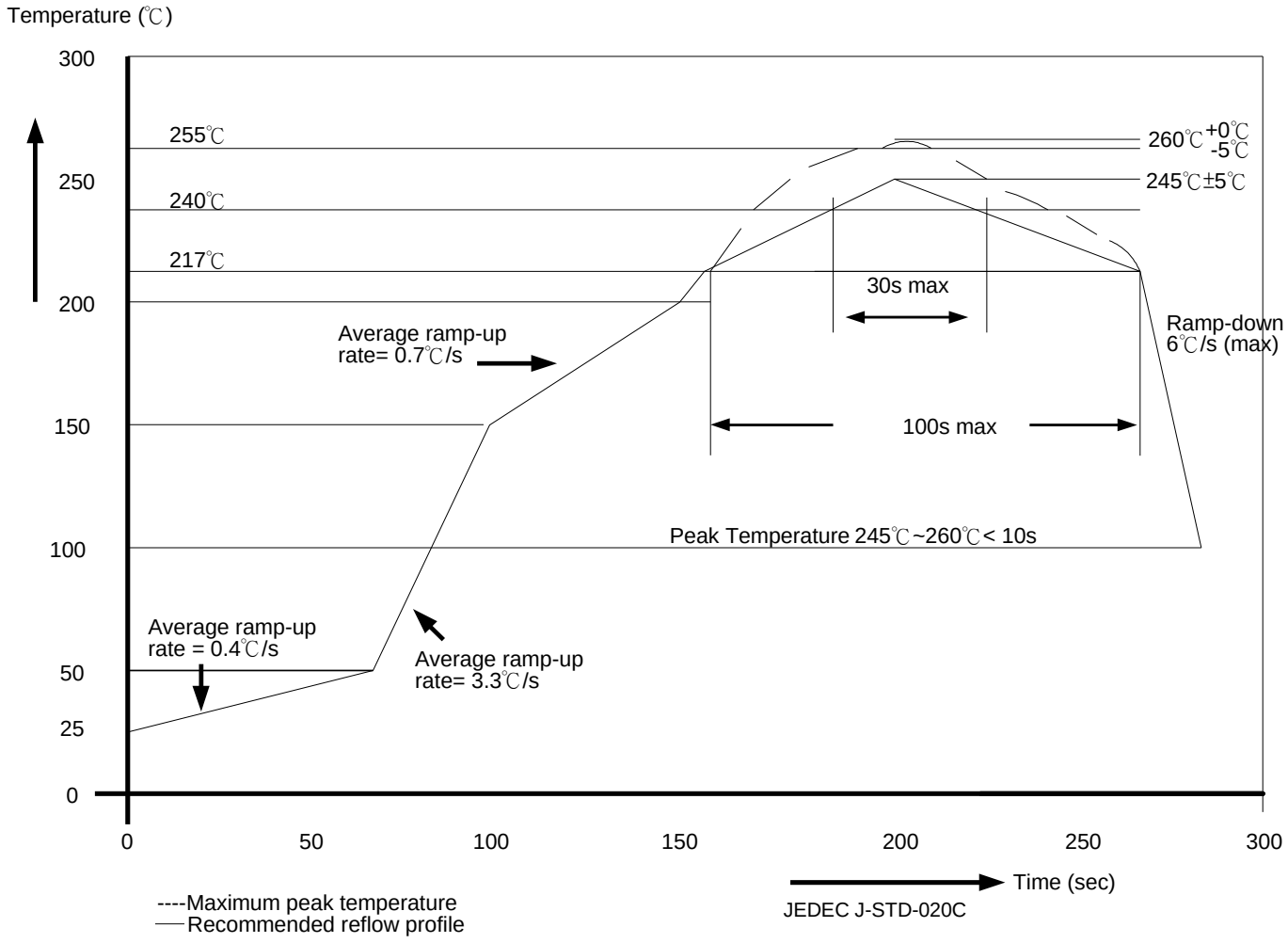
Switching Noise Reduction

The output ports of LED drivers are frequently switching in typical applications. This behavior usually causes switching noise due to the parasitic inductance on PCB. To eliminate switching noise, please refer to “Application Note for 8-bit and 16-bit LED Drivers-Overshoot”.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to reflow processes which adopt tin/lead (SnPb) solder paste. Please refer to JEDEC J-STD-020C for temperature setting. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.

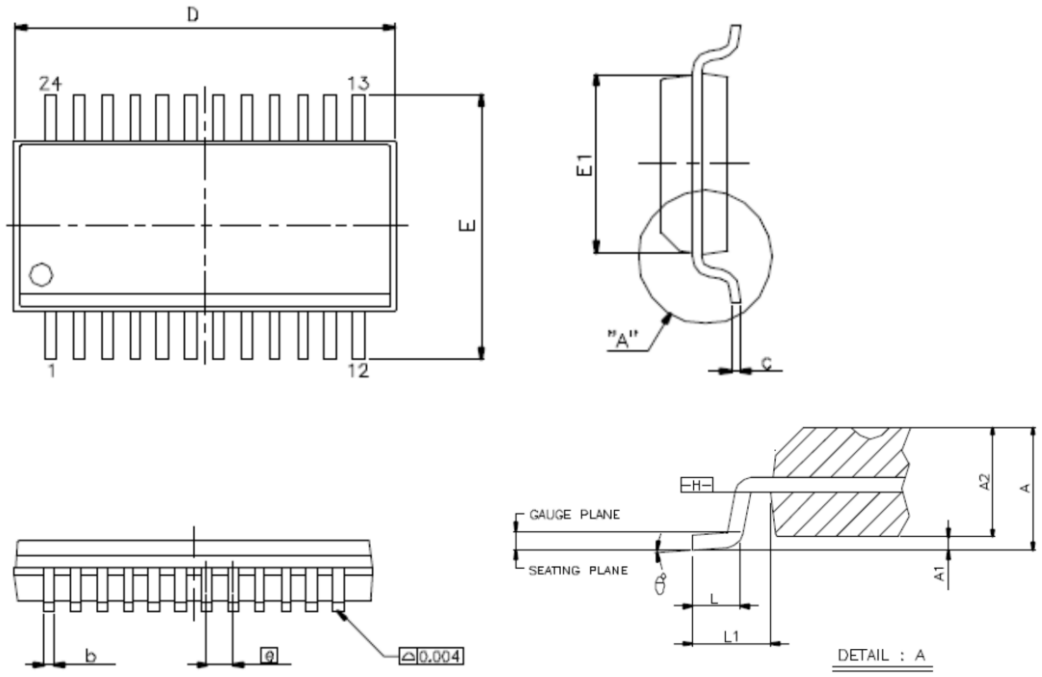
For managing MSL3 Package, it should refer to JEDEC J-STD-020C about floor life management & refer to JEDEC J-STD-033C about re-bake condition while IC's floor life exceeds MSL3 limitation.



Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

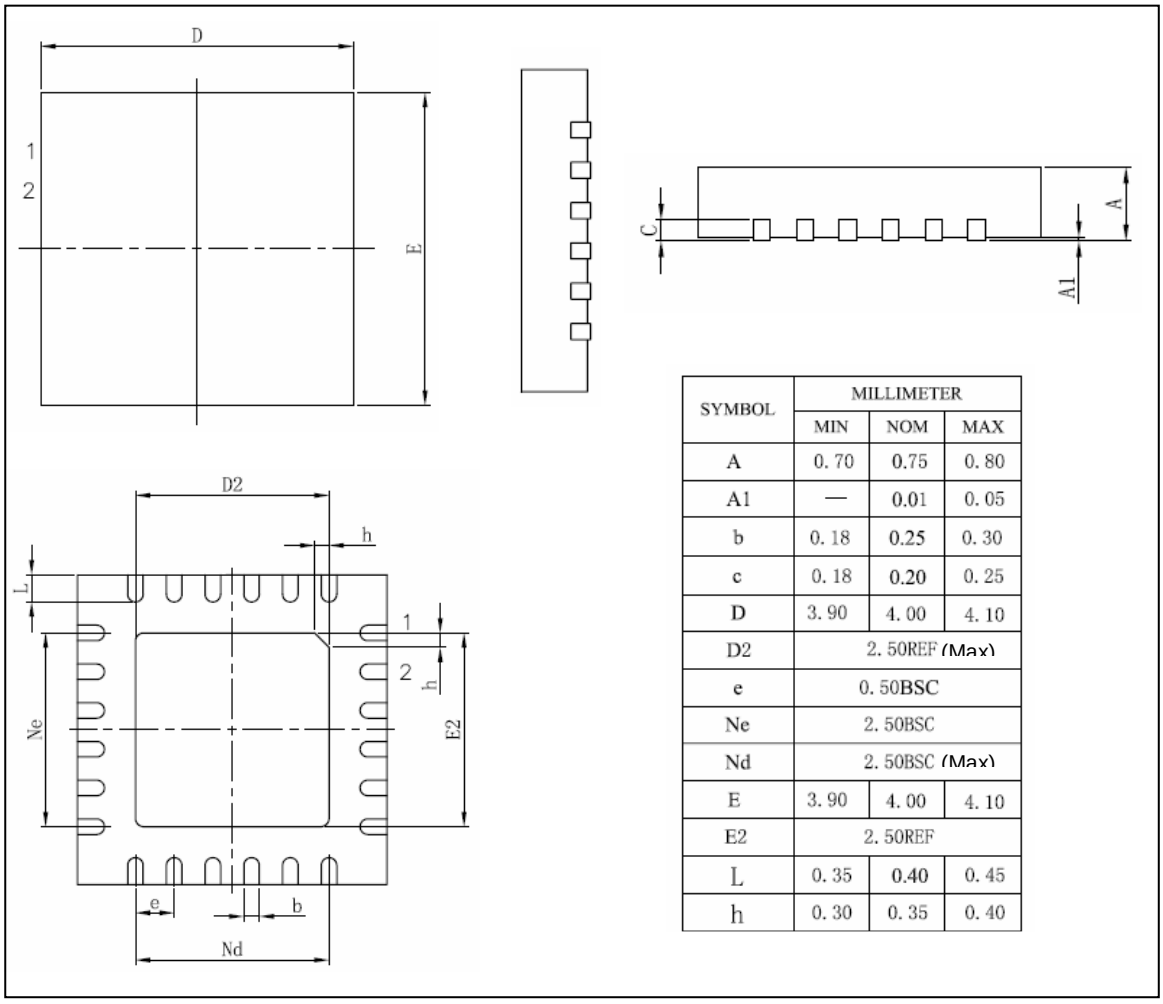
*For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
θ°	0	—	8	0	—	8

MBI6024GP Outline Drawing



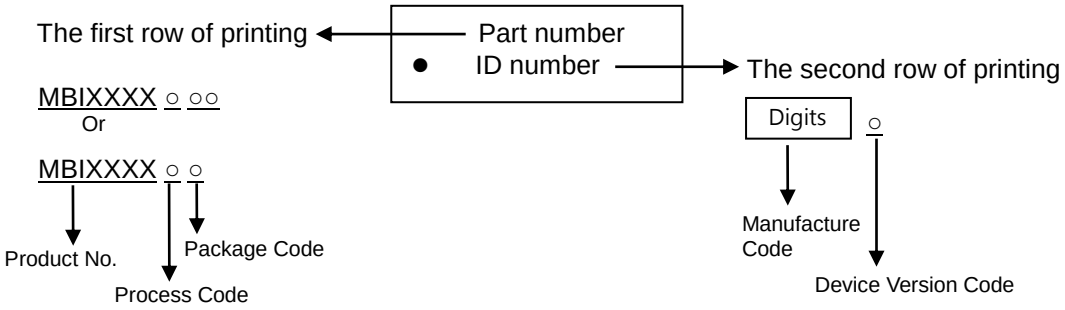
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.01	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	3. 90	4. 00	4. 10
D2	2. 50REF (Max)		
e	0. 50BSC		
Ne	2. 50BSC		
Nd	2. 50BSC (Max)		
E	3. 90	4. 00	4. 10
E2	2. 50REF		
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40

MBI6024GFN Outline Drawing

Note 1: The unit for the outline drawing is mm.

Note 2: Please use the maximum dimensions for the thermal pad layout. To avoid the short circuit risk, the vias or circuit traces shall not pass through the maximum area of thermal pad.

Product Top Mark Information



Product Revision History

Datasheet version	Device version code
V1.00	A
V1.01	A
V1.02	A
V2.00	B
VA.00	B
VB.00	C
VB.01	C

Product Ordering Information

Part Number	**RoHS-Compliant Package Type**	**Weight (g)**
MBI6024GP-C	SSOP24L-150-0.64	0.11
MBI6024GFN-C	QFN24L-4*4-0.5	0.0379

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