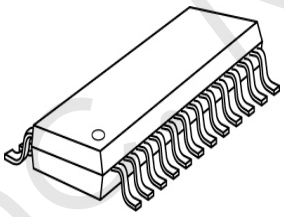
PWM-Embedded 3x4-Channel Constant-Current Sink Driver for LED Strips

Features

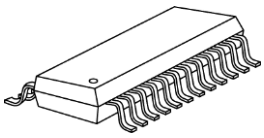
- Supply voltage
  - 6V to 24V by internal LDO
  - 3.3V / 5V direct input
- 3x4-channel constant-current sink driver for LED strips
  - Constant current range:
    3mA to 45mA @ V_{DD}=6 ~24V or V_{DD}=V_{CA}=5V
    3mA to 30mA @ V_{DD}=V_{CA}=3.3V
  - 3 groups of current gain
  - Sustaining voltage at output channels: 28V (max.)
- Embedded 16-bit PWM generator
  - Gray scale clock generated by the embedded oscillator
  - 16-bit S-PWM patented technology
- Reliable data transmission
  - Daisy-chain topology
  - Two-wire transmission interface
  - Phase-inversed output clock
  - Built-in buffer for long distance transmission
- Selectable output polarity to work as a PWM controller
- RoHS-compliant packages
  - SSOP-24
  - TSSOP-24
  - QFN-24

Shrink SOP



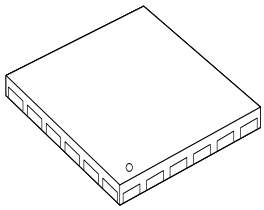
GP: SSOP24L-150-0.64

Thin Shrink SOP



GTS: TSSOP24L-173-0.65

Quad Flat No-Lead



GFN: QFN24L-4*4-0.5

Application

- LED strips
- Mesh display
- Architectural lighting

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Product Description

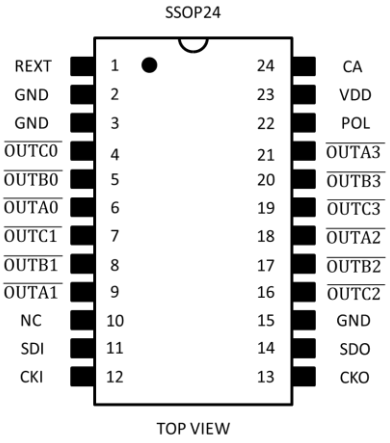
MBI6033 is a 3x4-channel, constant-current, PWM-embedded sink driver for LED strips. MBI6033 provides constant current ranging from 3mA to 45mA for each output channel and are adjustable through only single external resistor and corresponding current gain settings. Besides, MBI6033 supports 6V to 24V wide range power systems and sustains 28V at output channels.

With Scrambled-PWM (S-PWM) technology, MBI6033 enhances pulse width modulation by scrambling the “on” time into several “on” periods to increase visual refresh rate at the same gray scale performance. Besides, the gray scale clock (GCLK) is generated by the embedded oscillator. Moreover, MBI6033 provides 16-bit gray scale which provides 65,536 gray scales for each LED to enrich the color.

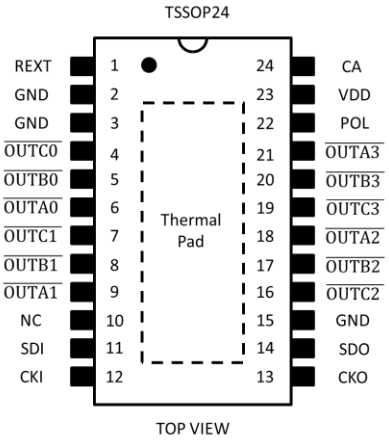
3 independent 7-bit current gain settings are built-in MBI6033, so the user can set independent output current for R/G/B LED by a single current set resistor and current gain instead of 3 current set resistors.

In addition, MBI6033 features a two-wire transmission interface to make cluster-to-cluster connection easier. To improve the transmission quality, MBI6033 provides phase-inversed output clock to eliminate the accumulation of signal pulse width distortion. MBI6033 adopts manual-synchronization to maintain the synchronization of image frames between ICs. MBI6033 has selectable polarity to drive high-power drivers or MOS as a PWM controller.

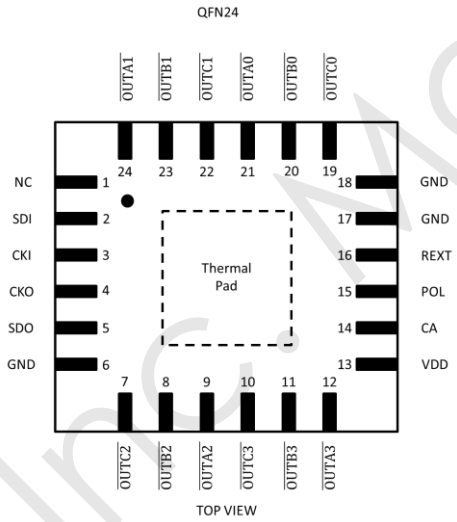
Pin Configuration



MBI6033GP



MBI6033GTS



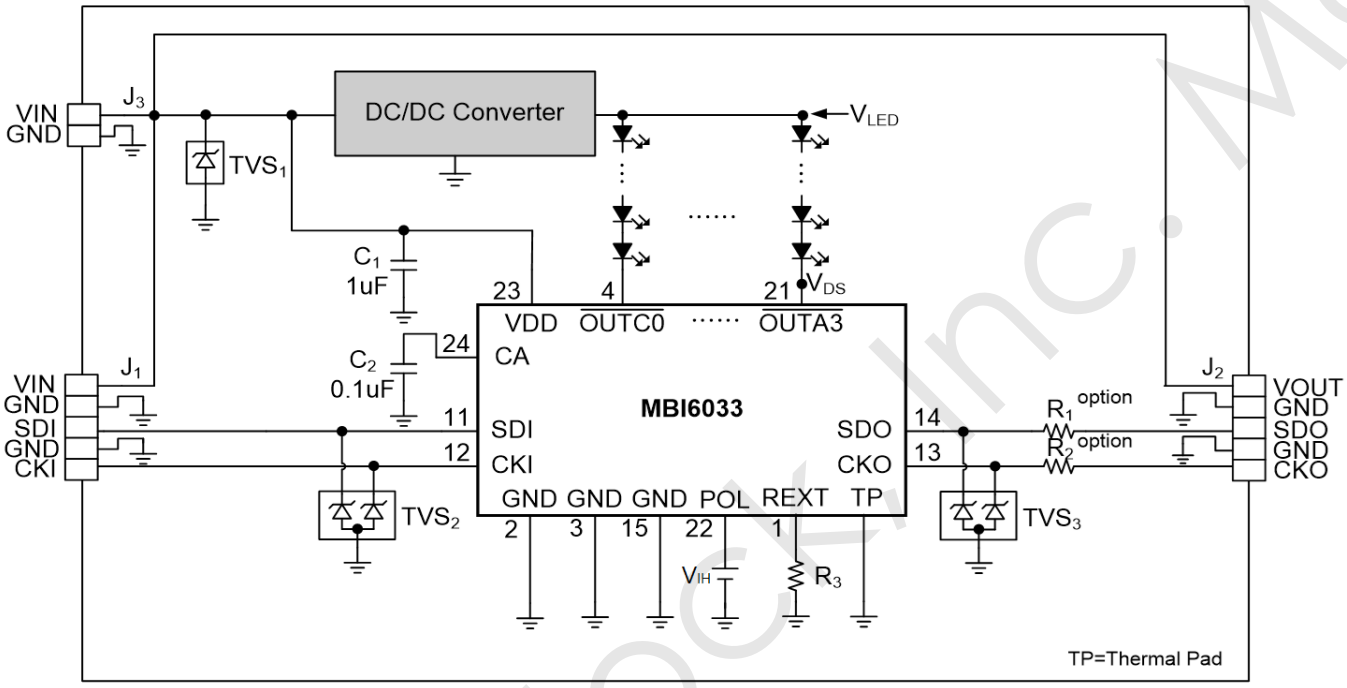
MBI6033GFN

Terminal Description

Pin			Names	Attribute	Description and function
GP	GTS*	GFN*			
1	1	16	REXT	O	Input terminals for setting output current by connecting to an external resistor
2, 3, 15	2, 3, 15	6, 17, 18	GND	P	Ground terminal
4, 5, 6	4, 5, 6	19, 20, 21	$\overline{OUTA0}$, $\overline{B0}$, $\overline{C0}$	O	Output terminals for constant-current output
7, 8, 9	7, 8, 9	22, 23, 24	$\overline{OUTA1}$, $\overline{B1}$, $\overline{C1}$	O	Output terminals for constant-current output
10	10	1	NC	-	Leave it unconnected
11	11	2	SDI	I	Input terminal for serial data input
12	12	3	CKI	I	Input terminal for clock input
13	13	4	CKO	O	Output terminal for clock output
14	14	5	SDO	O	Output terminal for serial data input
16, 17, 18	16, 17, 18	10, 11, 12	$\overline{OUTA2}$, $\overline{B2}$, $\overline{C2}$	O	Output terminals for constant-current output
19, 20, 21	19, 20, 21	7, 8, 9	$\overline{OUTA3}$, $\overline{B3}$, $\overline{C3}$	O	Output terminals for constant-current output
22	22	15	POL	I	For selecting output polarity POL pin = High → PWM mode (DCDC) 1. The output channel is high active 2. Only operable with none current gain mode. The command and input data type should be the same as without current gain. POL pin = Low (default) → constant current mode (LED) 1. The output channel is low active 2. Operable with or without current gain, the command and input data type should follows accordingly.
23	23	13	VDD	P	Input voltage, 3.3V/5V/6~24V
24	24	14	CA	O	Connecting a capacitor to GND to enhance the stability of CA
-	Thermal Pad	Thermal Pad	Thermal Pad	-	Heat dissipation pad*, please connect to GND

*The desired thermal conductivity will be improved on condition that a heat-conducting copper foil on PCB is soldered with thermal pad.

Typical Application Circuit

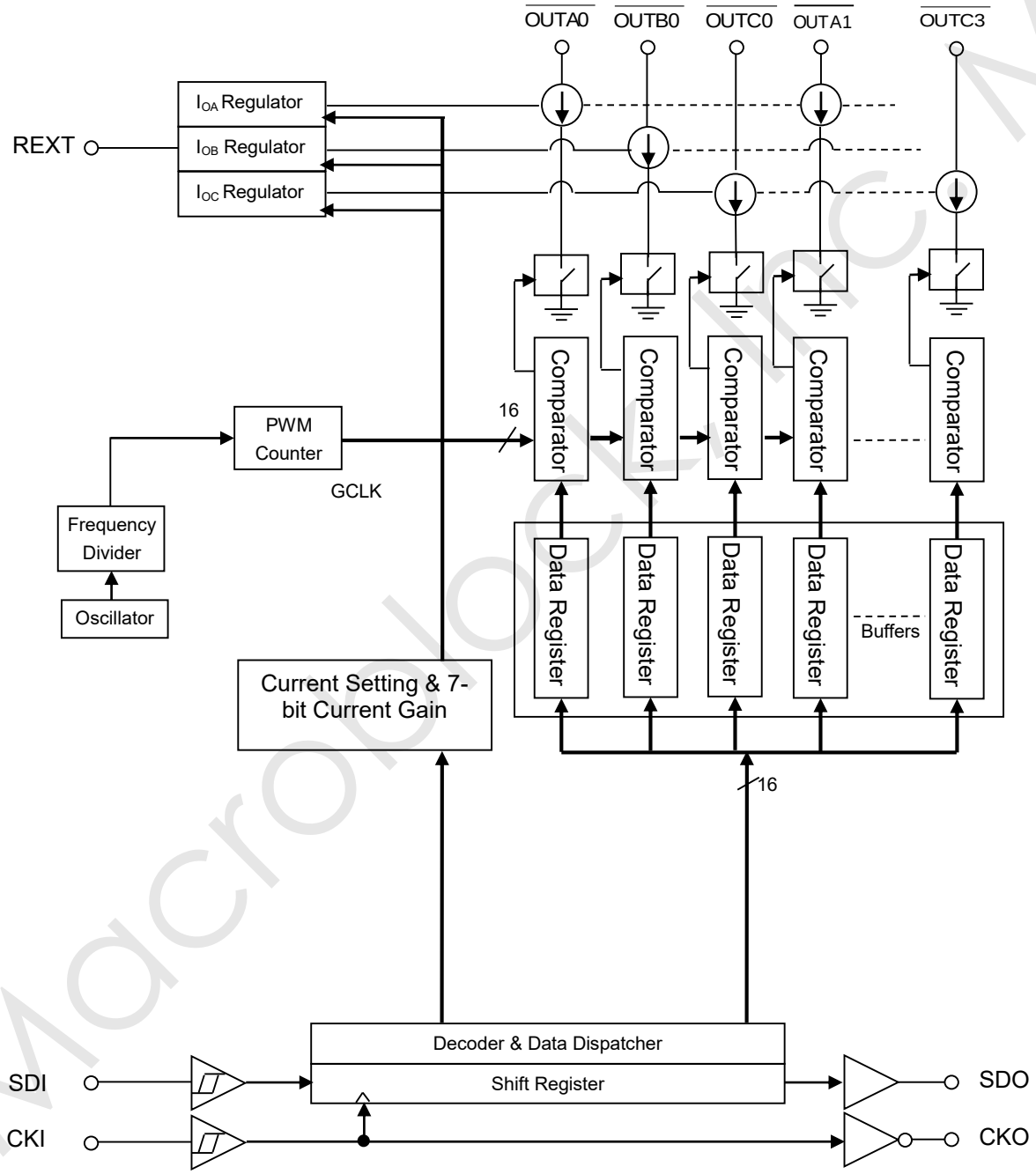


MBI6033GTS Application Circuit

Note:

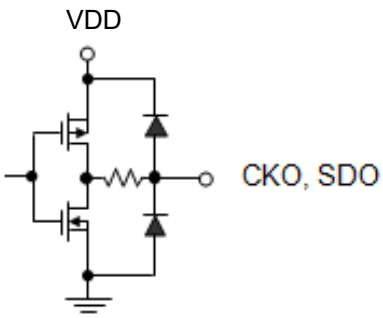
1. TVS_1~TVS_3 are Transient Voltage Suppressor (TVS).
2. C_1~C_2 are required. The values of the C_1~C_2 are reference only. Tantalum capacitors and Ceramic capacitors are recommended.
3. For hot plug, system grounding, connector design, external ESD protection, or detailed circuit information, please refer to the *"MBI6033 Application Note"* for detailed information.

Block Diagram

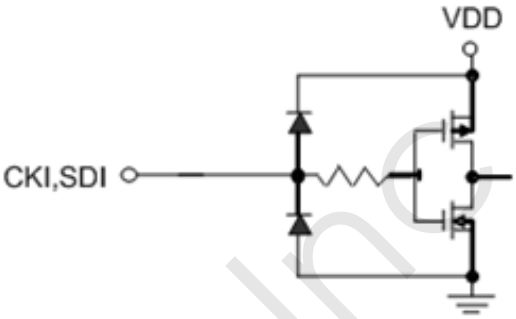


Equivalent Circuits of Inputs and Outputs

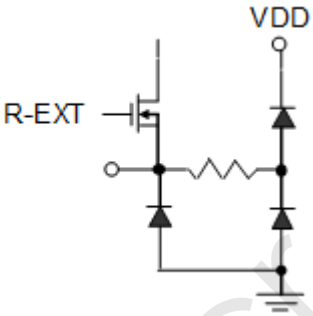
CKO、SDO terminals



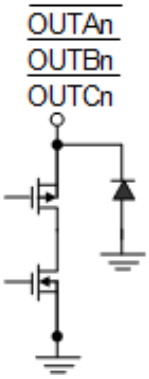
CKI、SDI terminals



REXT terminals



OUTAn、Bn、Cn termainal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0 ~ 28	V
LDO Output Voltage		V_{CA}	-0.4 ~ 5.5	V
Sustaining Voltage at CKI, SDI Pins		V_{IN}	-0.4 ~ V_{CA}+0.4	V
Sustaining Voltage at CKO, SDO Pins		V_{OUT}	-0.4 ~ V_{CA}+0.4	V
Sustaining Voltage at $\overline{OUTn}$ Pins		V_{DS}	-0.4 ~ +28	V
Output Current per Output Channel		I_{OUT}	+50	mA
GND Terminal Current		I_{GND}	630	mA
Heat dissipation (On 4-Layer PCB, Ta=25°C)*	GP	P_D	1.65	W
	GTS	P_D	2.01	W
	GFN	P_D	3.03	W
Thermal Resistance (By simulation, on 4-Layer PCB)*	GP	$R_{th(j-a)}$	72.7	°C/W
	GTS	$R_{th(j-a)}$	59.6	°C/W
	GFN	$R_{th(j-a)}$	39.5	°C/W
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40 ~ +85	°C
Storage Temperature		T_{stg}	-55 ~ +150	°C
ESD Rating	Human Body Mode (MIL-STD-883G Method 3015.8)	HBM	Class 3A (5KV)	-
	Machine Mode (ANSI/ ESD S5.2-2009)	MM	Class M4 (400V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. Users should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=6.0~24.0V or V_{DD}=V_{CA}=5V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		6	-	24	V
			V_{DD}=V_{CA}		4.5	5	5.5	
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUTAn}$ ~ $\overline{OUTCn}$ = Off		-	-	28	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		3	-	45	mA
Driving Current		I_{OH}	CKO, SDO at V_{OH} = V_{CA} - 0.2V		1.0	1.8	-	mA
		I_{OL}	CKO, SDO at V_{OH} = 0.2V		1.0	1.8	-	mA
Output Leakage Current		I_{OUT}	V_{DS} = 28.0V, $\overline{OUTAn}$ ~ $\overline{OUTCn}$ = Off		-	-	1.0	μA
Current Skew (Channel)		dI_{OUT1}	I_{OUT} = 20mA, V_{DS} = 1.0V	R_{ext}=1.8KΩ	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT} = 20mA, V_{DS} = 1.0V	R_{ext}=1.8KΩ	-	±1.5	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.5	%/V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 6V and 24V		-	±1.0	±2.0	%/V
Input Voltage of CKI and SDI Pins	"H" level	V_{IH}	-		0.8 x V_{CA}	-	V_{CA}	V
	"L" level	V_{IL}	-		GND	-	0.2 x V_{CA}	V
Output Voltage of CKO and SDO Pins	"H" level	V_{OH}	I_{OH} = +1.8mA		V_{CA} - 0.2	-	-	V
	"L" level	V_{OL}	I_{OL} = -1.8mA		-	-	0.2	V
Voltage at R-EXT		V_{REXT}	$\overline{OUTAn}$ ~ $\overline{OUTCn}$ =On		0.57	0.60	0.63	V
Knee Voltage*		V_{Knee}	-		-	-	1.2	V
Supply Current**	"Off"	I_{DD}(off)	All channel off, REXT open		1.5	3	4.5	mA
			All channel off R_{ext}=1.8KΩ, IOUT=20mA CKI, SDI=Low, CKO, SDO=NC,		5	7	9	
	"On"	I_{DD}(on)	R_{ext}=1.8KΩ, IOUT=20mA CKI, SDI=Low, CKO, SDO=NC, All channel on		6	8	9	
			R_{ext}=1.8KΩ, IOUT=20mA CKI=10MHz, CKO, SDO=NC, All channel on		8	10	12	

*One channel turns on.

** The supply current may vary with the loading conditions.

Electrical Characteristics (V_{DD}=V_{CA}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	V_{DD}=V_{CA}		3.0		3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUTAn}$ ~ $\overline{OUTCn}$ = Off		-	-	28.0	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		3	-	30	mA
Driving Current		I_{OH}	CKO, SDO at V_{OH}=V_{CA}-0.2V		1.0	1.8	-	mA
		I_{OL}	CKO, SDO at V_{OH}=0.2V		1.0	1.8	-	mA
Output Leakage Current		I_{OUT}	V_{DS} = 28.0V, $\overline{OUTAn}$ ~ $\overline{OUTCn}$ = Off		-	-	1.0	μA
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=1.8KΩ	-	±1.5	±3.0	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=20mA V_{DS}=1.0V	R_{ext}=1.8KΩ	-	±1.5	±6.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	±0.5	%/V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 3.0V and 3.6V		-	±1.0	±2.0	%/V
Input Voltage of CKI, SDI Pins	"H" level	V_{IH}	-		0.8 x V_{CA}	-	V_{CA}	V
	"L" level	V_{IL}	-		GND	-	0.2 x V_{CA}	V
Output Voltage of CKO, SDO Pins	"H" level	V_{OH}	I_{OH} = +1.8mA		V_{CA} - 0.2	-	-	V
	"L" level	V_{OL}	I_{OL} = -1.8mA		-	-	0.2	V
Voltage at R-EXTA,B,C Pins		V_{REXT}	$\overline{OUTAn}$ ~ $\overline{OUTCn}$ =On		0.57	0.60	0.63	V
Knee Voltage*		V_{Knee}	-		-	1.0	1.2	V
Supply Current**	"Off"	I_{DD}(off)	All channel off, REXT open		1.5	3	4.5	mA
			All channel off R_{ext}=1.8KΩ, IOUT=20mA CKI, SDI=Low, CKO, SDO=NC,		5	7	9	
	"On"	I_{DD}(on)	R_{ext}=1.8KΩ, IOUT=20mA CKI, SDI=Low, CKO, SDO=NC, All channel on		6	8	9	
			R_{ext}=1.8KΩ, IOUT=20mA CKI=10MHz, CKO, SDO=NC, All channel on		8	10	12	

*One channel turns on.

**The supply current may vary with the loading conditions.

Switching Characteristics (V_{DD}=6.0~24.0V; V_{CA}=V_{DD}=5V, Ta=25°C)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation delay time (“H” to ”L” or “L” to “H”)	CKI↑-CKO↓	t_{P1}	Test condition: VLED =4V VDS = 1V IOUT=20mA R_{ext}=1.8KΩ R_L =150Ω C_L = 10pF C_1 = 4.7uF C_2 = 0.1uF C_3 = 4.7uF	11	16	21	ns
	CKO↓-SDO	t_{P2}		15	25	35	ns
	SDI(n+1) – SDO(n)	t_{P3}		wd*	wd*	wd*	ns
	CKI(n) – CKI(n+1)	t_{P4}		t_{P1}+ wd*	t_{P1}+ wd*	t_{P1}+ wd*	ns
	CKO↓-SDI	t_{P5}		15	25	35	ns
Rise Time	CKO/SDO/SDI	t_{OR}		2	5	8	ns
	$\overline{OUTA}$ ~ $\overline{OUTC}$	t_{OR1}		10	20	30	ns
Fall Time	CKO/SDO/SDI	t_{OF}		2	5	8	ns
	$\overline{OUTA}$ ~ $\overline{OUTC}$	t_{OF1}		20	30	40	ns
Hold Time	SDI-CKI↓	$t_{H(D)}$		8	-	-	ns
Setup Time	CKI↓-SDI	$t_{S(D)}$		8	-	-	ns
Pulse Width	CKI	t_W		15	-	-	ns
Frequency	CKI	F_{CKI}	Flat(AWG26), 50cm distance	0.2	-	10	MHz
	PWM clock	F_{PCKL}	-	8.0	10	12.0	MHz
	Internal oscillator	-	-	8.0	10	12.0	MHz
Timeout period**		$t_{timeout}$	-	21	-	-	μs

Note:

* wd: is wire delay , which is dependent on wire distance and wire material.

**The period of internal OSC is 8MHz (min.) ~ 12MHz (max.), so the time-out period is 168x83.3ns (13.9μs) ~ 168x125ns (21μs).

***The Gray Scale Clock Frequency is 12MHz (max.) when the GCLK=frequency of internal oscillator.

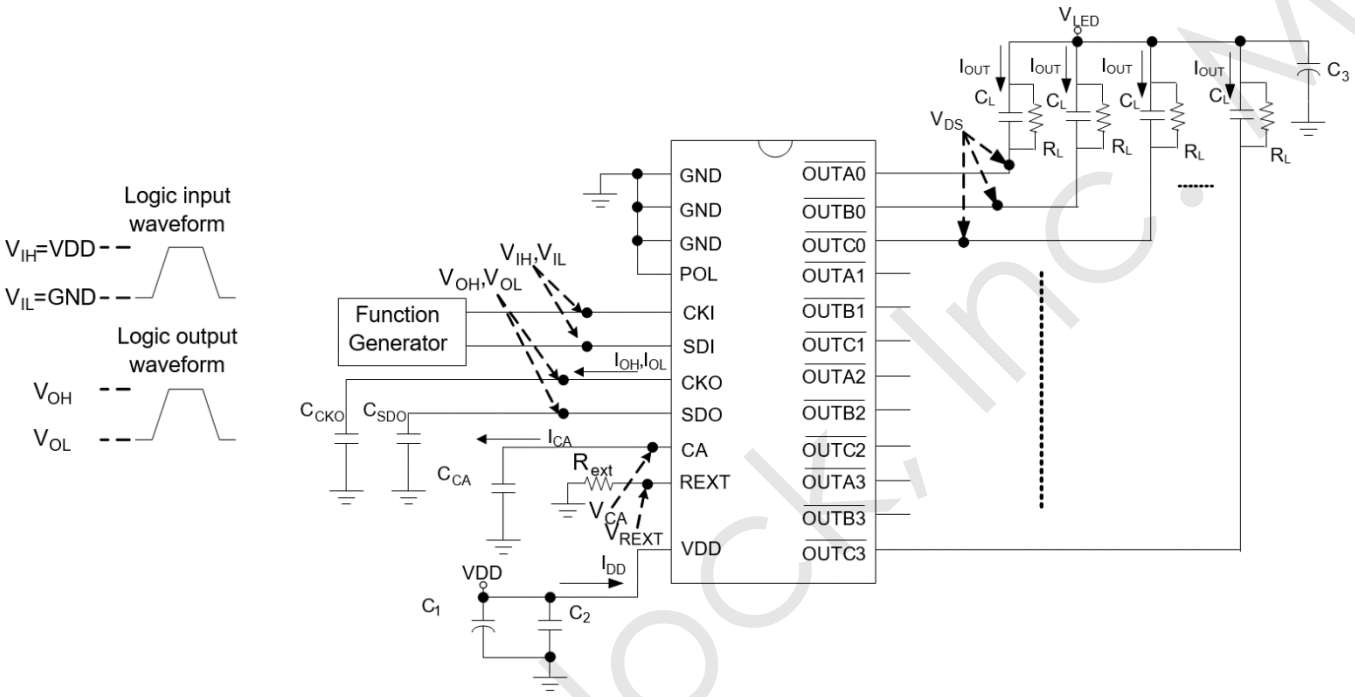
****The maximum frequency may be limited by different application conditions. Please refer to the application note for details.

Switching Characteristics (V_{DD}=V_{CA}=3.3V, Ta=25˚C)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation delay time (“H” to ”L” or “L” to “H”)	CKI↑-CKO↓	t_{P1}	Test condition: VLED =4V VDS = 1V IOUT = 20mA Rext = 1.8KΩ R_L =150ohm C_L = 10pF C_1 = 4.7uF C_2 = 0.1uF C_3 = 4.7uF C_{ca} = 0.1uF	18	23	28	ns
	CKO↓-SDO	t_{P2}		20	30	40	ns
	SDI(n+1) – SDO(n)	t_{P3}		wd*	wd*	wd*	ns
	CKI(n) – CKI(n+1)	t_{P4}		t_{P1}+ wd*	t_{P1}+ wd*	t_{P1}+ wd*	ns
	CKO↓-SDI	t_{P5}		20	30	40	ns
Rise Time	CKO/SDO/SDI	t_{OR}		2	5	8	ns
	$\overline{OUTA}$ ~ $\overline{OUTC}$	t_{OR1}		10	20	30	ns
Fall Time	CKO/SDO/SDI	t_{OF}		2	5	8	ns
	$\overline{OUTA}$ ~ $\overline{OUTC}$	t_{OF1}		30	50	70	ns
Hold Time Setup Time	SDI-CKI↓	$t_{H(D)}$		10	-	-	ns
	CKI↓-SDI	$t_{S(D)}$		10	-	-	ns
Pulse Width	CKI	t_W		15	-	-	ns
Frequency	CKI	F_{CKI}	Flat(AWG26), 50cm distance	0.2	-	10	MHz
	PWM clock	F_{PCKL}	-	10.0	12.0	14.0	MHz
	Internal oscillator	-	-	10.0	12.0	14.0	MHz
Timeout period**		$t_{timeout}$		16.8	-	-	μs

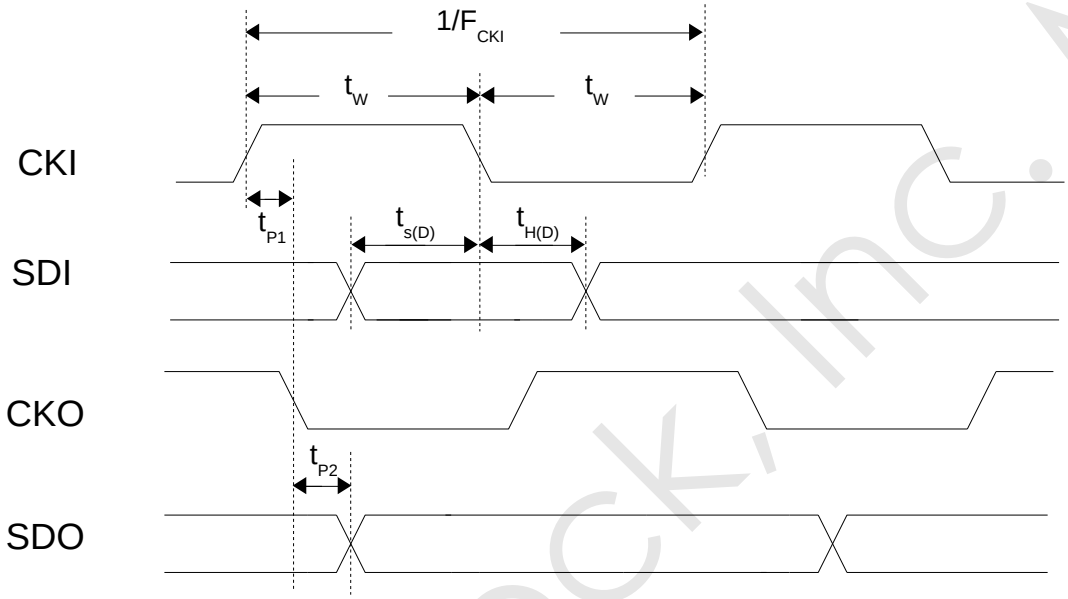
Note:
* wd: is wire delay , which is dependent on wire distance and wire material.
**The period of internal OSC is 10MHz (min.) ~ 14MHz (max.), so the time-out period is 168x71.42ns (12μs) ~ 168x100ns (16.8μs).
***The Gray Scale Clock Frequency is 14MHz (max.) when the GCLK=frequency of internal oscillator.
****The maximum frequency may be limited by different application conditions. Please refer to the application note for details.

Test Circuit for Electrical / Switching Characteristics

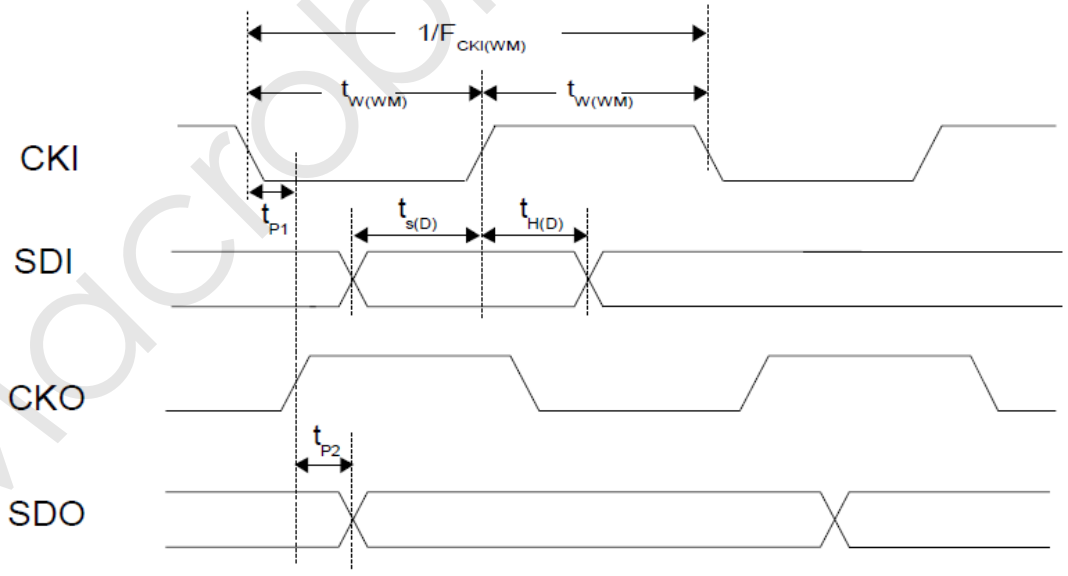


Timing Waveform

Write mode for even IC



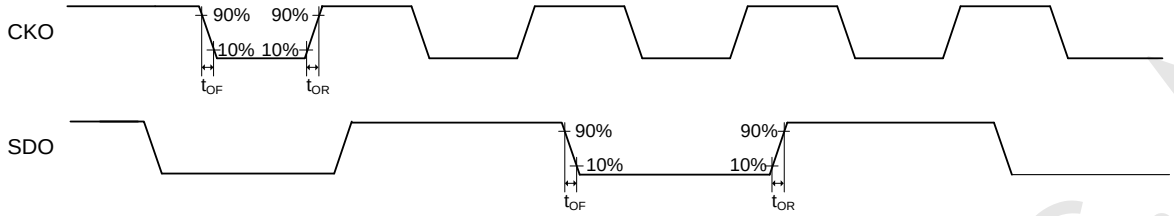
Write mode for odd IC



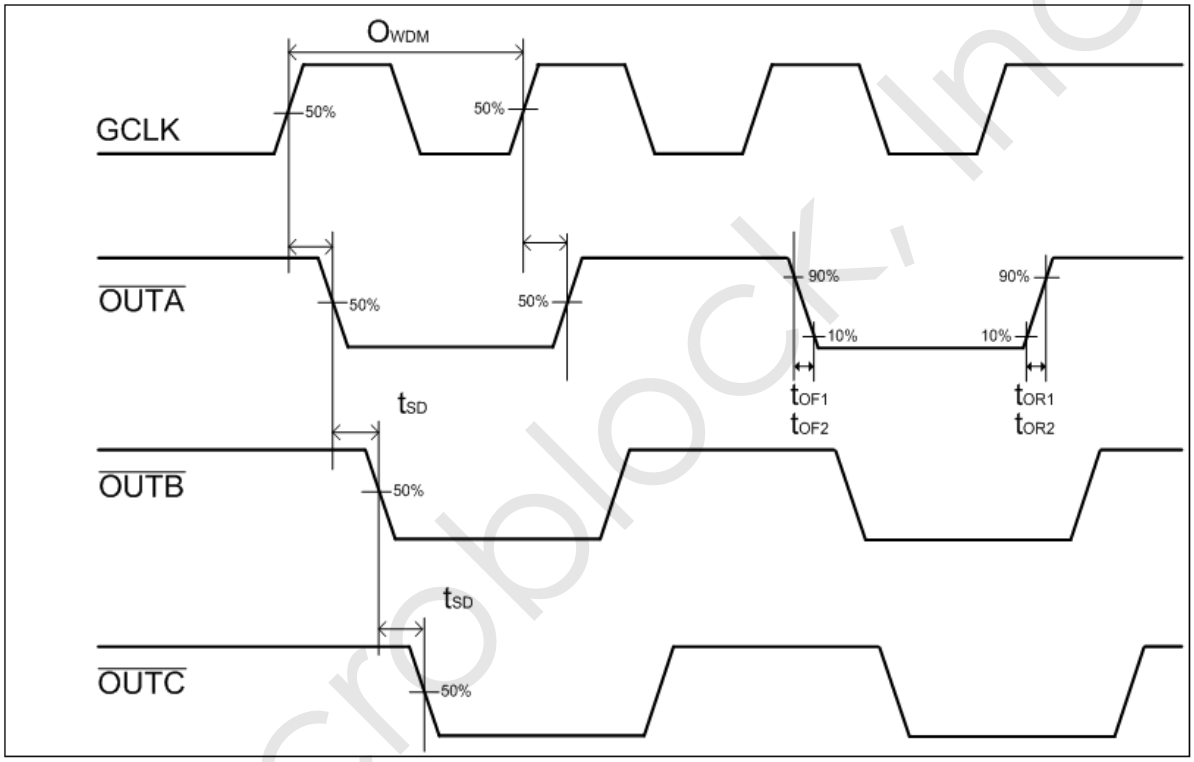
Note:
Even IC means 0th, 2nd , 4th, … IC connected to controller
Odd IC means 1st, 3rd, 5th … ICs connected to controller

Output Timing

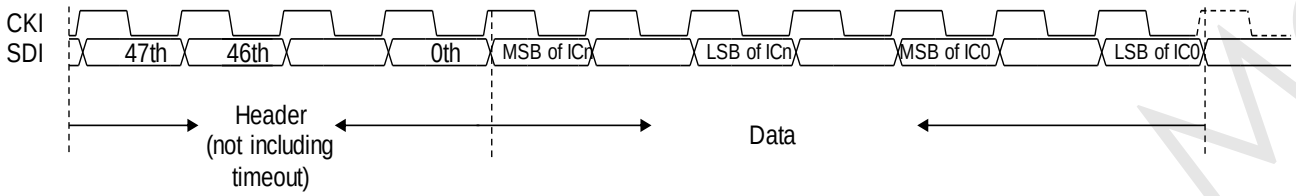
TOF / TOR



TOF1 / TOR1



Data programming sequence

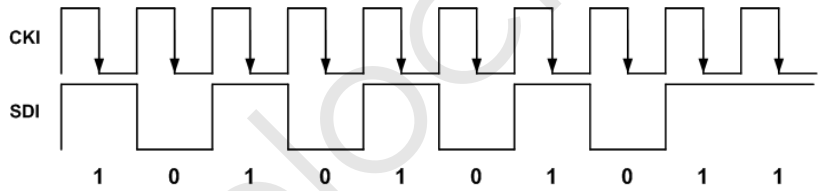


The above figure shows an application example of MBI6033. The drivers are connected serially and the data sequence sent by the controller is shown in above figure. All commands are composed of “Header” and “Data”, as shown in the above figure.

The programming data sequence is from ICn, ICn-1, … to IC0 and for each IC, MSB bit is sent first.

(Please also refer to sec. of “The structure of data packet”)

Control Interface



MBI6033 adopts the SPI-like interface (CKI/SDI). By SPI-like interface, MBI6033 samples the data (SDI) at the falling edge of the clock (CKI).The above waveform is the example of the SPI-like interface.

Principle of Operation

MBI6033 receives the data packet containing targeted gray scale data from the controller, and turns on the output channels according to the gray scale data. The gray scale clock of PWM generator, GCLK, is generated by the embedded oscillator. MBI6033 provides SPI-like interface (CKI, SDI), a two-wire only transmission interface, to address the data, so that MBI6033 receives the data directly without latching data.

Input Voltage Regulation

MBI6033 integrates a LDO which can convert 6~24V input voltage to 5V to supply the internal circuit. A user can connect a capacitor in CA pin to compensate LDO. Although CA is an output pin, the driving current is very tiny. Do not use the output of CA pin to drive any device. If a user would like to power MBI6033 by regulated 5V or 3.3V, connect both V_{DD} and CA pins to regulated 5V or 3.3V.

Grayscale Control

MBI6033 provides 16-bit S-PWM grayscale mode to 64 segments, so that the visual refresh rate can be increased. For example, with S-PWM, the default PWM clock frequency is 10 MHz (VDD = 6V ~ 24V or VDD = Vca = 5V), the visual refresh rate of 16-bit grayscale mode will be increased to (10 MHz / 65,536) x 64 = 9.766 KHz

MBI6033 continuously repeats the PWM cycle and turns on the output ports according to the image data until the next image data is correctly recognized. Once the next input data is correctly recognized, MBI6033 will stop the present PWM cycle and restart a new PWM cycle to show the new data immediately.

16-bit grayscale data

The following is the equation for the duty cycle of output in 16-bit grayscale mode.

$$\text{The duty cycle of output (\%)} = \frac{\text{16-bit gray scale data}}{65536} \times 100\%$$

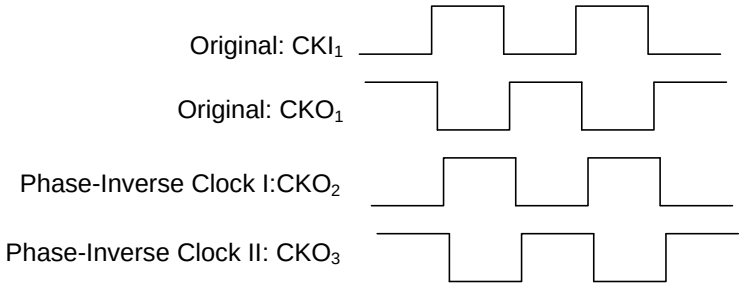
According to the above equation, the following table shows the examples:

16-bit gray mode scale output result

Example	Grayscale data	Duty Cycle of Output
1	65,535	99.9%
2	32,768	50%
3	16,384	25%
	. . .	. . .

Phase-inversed Output Clock

MBI6033 enhances the capability of cascading MBI6033 by phase-inversed output clock function. By phase-inversed output clock, the clock phase will be inversed from CKI to CKO to eliminate the accumulation of the pulse width deviation. This improves the signal integrity of data transmission. The following chart illustrates the phase-inversed output clock results.



The Structure of Data Packet

MBI6033's data packet contains three parts:

1. Prefix:
   The prefix is a symbol of "Silent-to-Reset", i.e. a time period for MBI6033 to distinguish two data packets.
2. Header:
   The header defines the cascaded IC numbers and also contains a command to decide the data type.
3. Data:
   This is the data for each IC. It may be gray scale data, dot correction data, or configuration data.

Structure of a data packet:

Prefix	Header	Data

Prefix

MBI6033 identifies the data as a new packet after time-out. Then users can follow the "time-out" protocol (time-out duration: stop t_{tout} + 1CKI + stop t_{tout}) to re-start packet decoding scheme.

If both CKI and SDI are tied-low and stop for more than the setting of CKI time-out period, MBI6033 will start to check the valid command of the next data packet. The prefix between two data packets helps MBI6033 identify the data packet correctly. The following timing diagram illustrates the interval between two data packets in 16-bit gray scale mode.

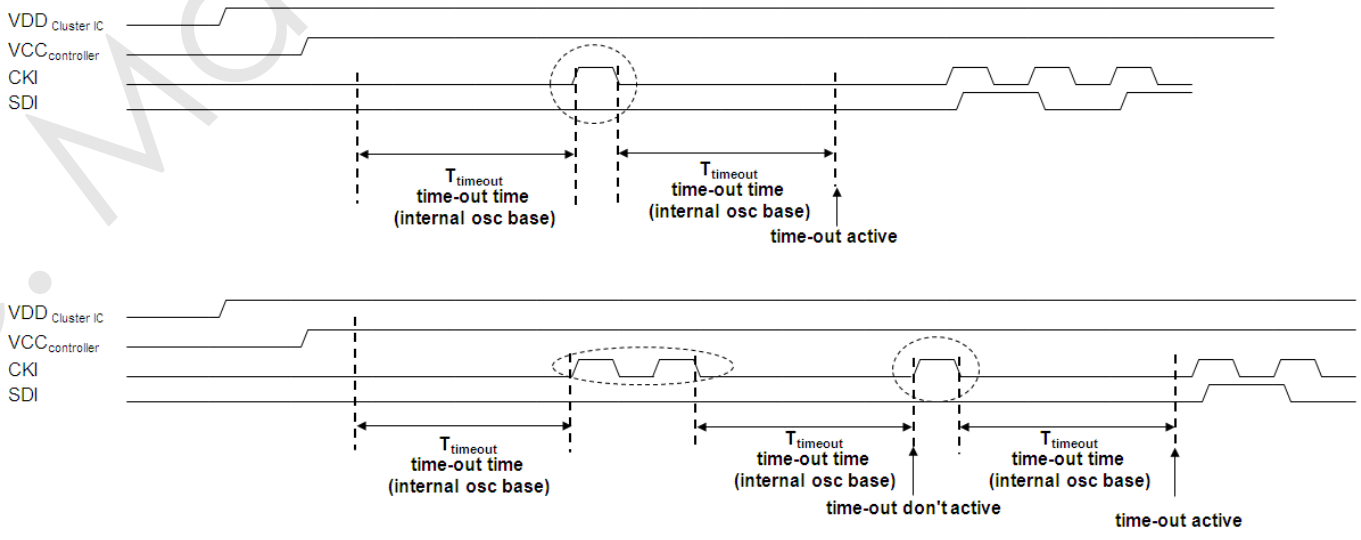
Time-out reset is to prevent ICs from misreading during the data transmission. The procedure is described below,

→ The CKI should be tied-low and stop for more than time-out period

→ One CKI pulse (SDI keep)

→ CKI should be tied-low and stop for more than time-out period.

Where the time-out period is at least 21 μs.



Setting the Data Types by the Command

MBI6033 provides three kinds of commands and input data types shown as the table below:

Command H[7:0]	Data Type
8'b11010101	Current gain mode
8'b11110011	Non-current gain mode
8'b11000001	Software reset

Once MBI6033 receives the SDI=1 (1'b1), MBI6033 will start to check if the data is a valid command or not. If the 8-bit data is a valid command, the driver will latch the specific data according to the protocol. If the 8-bit data is not a valid command, MBI6033 will wait for another SDI=1 (1'b1) to check the validity of the next command.

Time-Out Reset for Transmission Abort

Time-out reset is to prevent ICs from misreading during the data transmission. The procedure is described below,

→ The CKI should be tied-low and stop for more than time-out period

→ One CKI pulse (SDI keep)

→ CKI should be tied-low and stop for more than time-out period.

Where the time-out period is at least 21 μs.

Header Packet Format

48-bit header

Bit	Definition	Value	Function
47:40	H[7:0]	8'b11010101	Grayscale mode with current gain
		8'b11110011	Grayscale mode without current gain
39:26	S[13:0]	14'b00000000000000	Wait counter data. Always send 14'b 00000000000000
25:12	L[13:0]	N -1 N=Number of IC in series 14'bxxxx0000000000 ~ 14'bxxxx1111111111	Set the number of IC in series. The L[13:10] don't care. Only the L[9:0] are effective. For example: if we have 3 IC's in cascade, Length[13:0]=14'b0000 0000 0000 10
11:4	CF[7:0]	8'b00000000~8'b11111111	The configuration data. 8'b00000000 (default)
3:0	X1[3:0]	4'b0000	Reserved. Please keep "0000"

Configuration Mode

	MSB							LSB
Bit	11	10	9	8	7	6	5	4
Default Value	0	000			00		0	0

Bit	Definition	Value	Function
11	Reserved	1'b0	The value is suggested to be "0"
10:8	GCLK frequency	000 (default)	GCLK=frequency of internal oscillator, i.e. 10MHz (typ.)
		3'b001	GCLK=frequency of internal oscillator divided by 2, i.e. 5MHz (typ.)
		3'b 010	GCLK=frequency of internal oscillator divided by 4, i.e. 2.5MHz (typ.)
		3'b 011	GCLK=frequency of internal oscillator divided by 8, i.e. 1.25MHz (typ.)
		3'b 100	GCLK=frequency of internal oscillator divided by 16, i.e. 625KHz (typ.)
		3'b 101	GCLK=frequency of internal oscillator divided by 64, i.e. 156.25KHz (typ.)
		3'b 110	GCLK=frequency of internal oscillator divided by 128, i.e. 78.125KHz (typ.)
		3'b 111	GCLK=frequency of internal oscillator divided by 256, i.e. 39.0625KHz (typ.)
7:6	Reserved	2'b00	Reserved. Please keep "00"
5	Output turn-on	1'b0	Turn-on the output "1", all constant-current outputs (OUTC3-OUTA0) are controlled by the GS PWM timing controller. "0"', all constant-current outputs are forced off and PWM counter is reset to "0". Note: when this bit is from "0" to "1", PWM counter will be reset.
4	Reserved	1'b0	Reserved. Please keep "0"

Current Gain

24-bit current gain data

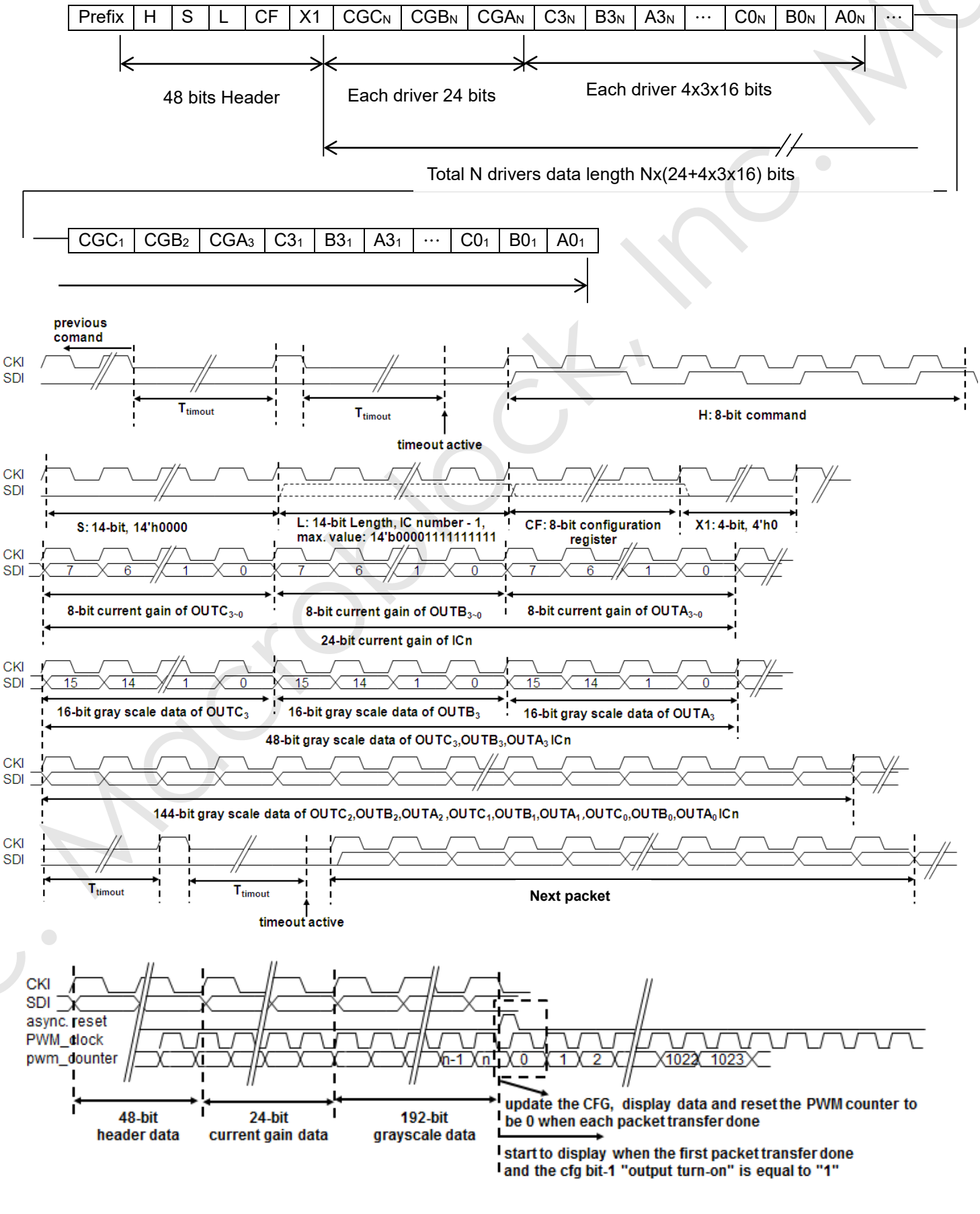
Bit	Definition	Value	Function
23:16	CGC_N[7]	1'b0	Reserved. Please keep "0"
	CGC_N[6:0]	7b'0000000~ 7b'1111111	The CGC_N[6:0] are 7 bits current gain data of Nth driver for $\overline{OUTC}$.
15:8	CGB_N[7]	1'b0	Reserved. Please keep "0"
	CGB_N[6:0]	7b'0000000~ 7b'1111111	The CGB_N[6:0] are 7 bits current gain data of Nth driver for $\overline{OUTB}$.
7:0	CGA_N[7]	1'b0	Reserved. Please keep "0"
	CGA_N[6:0]	7b'0000000~ 7b'1111111	The CGA_N[6:0] are 7 bits current gain data of Nth driver for $\overline{OUTA}$.

192-bit gray scale data

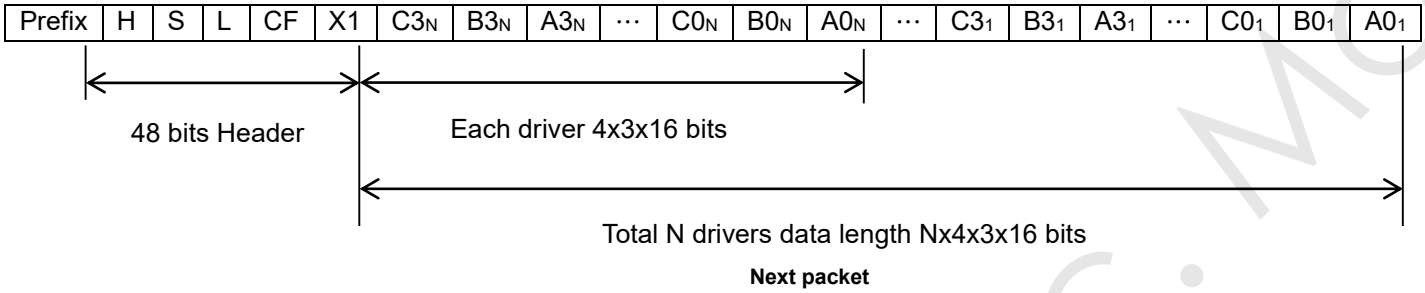
Bit	Definition	Value	Function
191:0	$C3_N$[15:0]~ $A0_N$[15:0]	Each channel is 16-bit. 16'h0000 ~ 16'hffff	16-bit x 12 channels gray scale data of the Nth driver. The data of $\overline{OUTC}_{3N}$ is sent first.

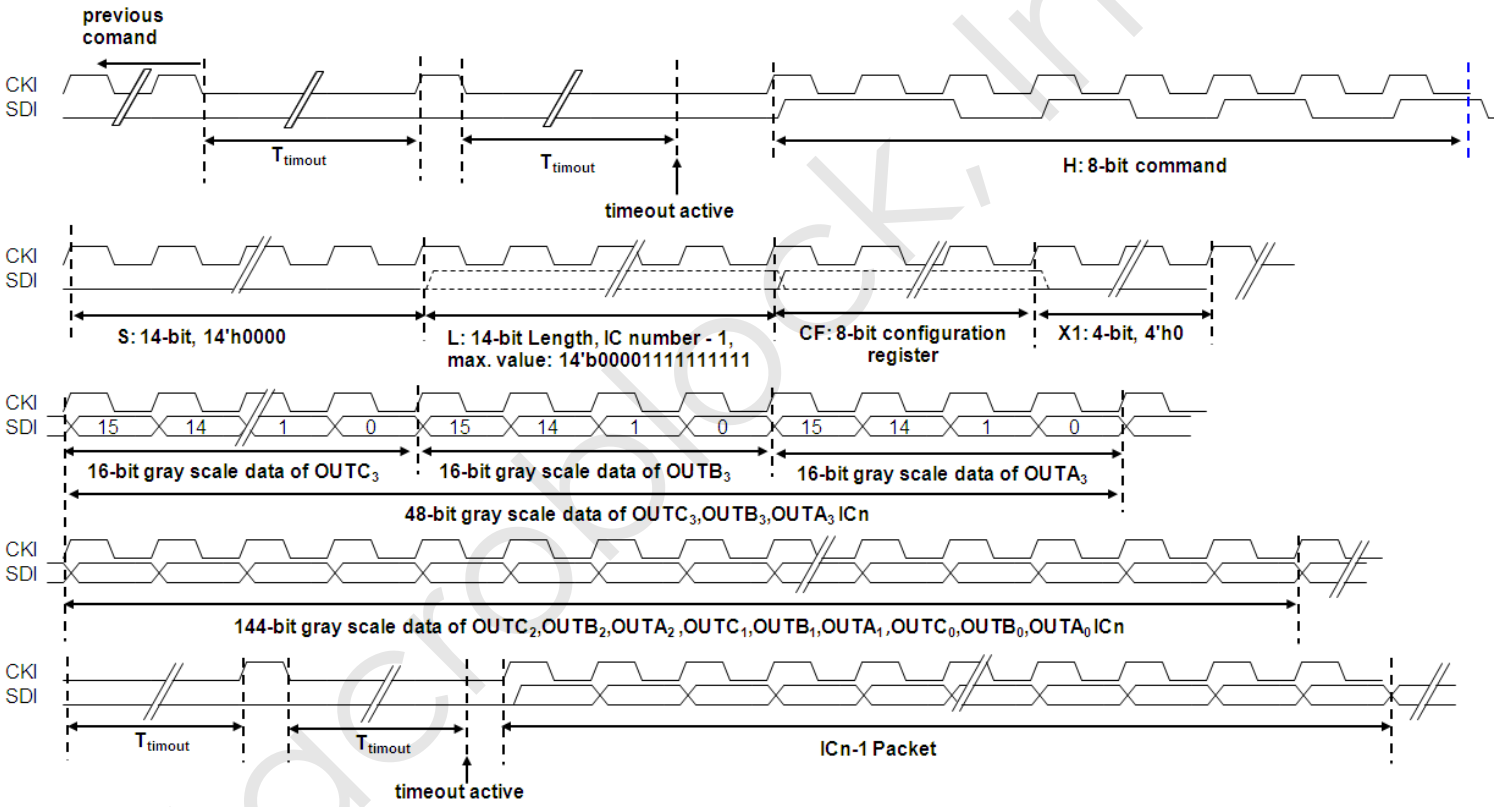
The gray scale data of the last IC is sent first, followed by the previous ICs, and the first IC's gray scale data is sent in the end of the packet.

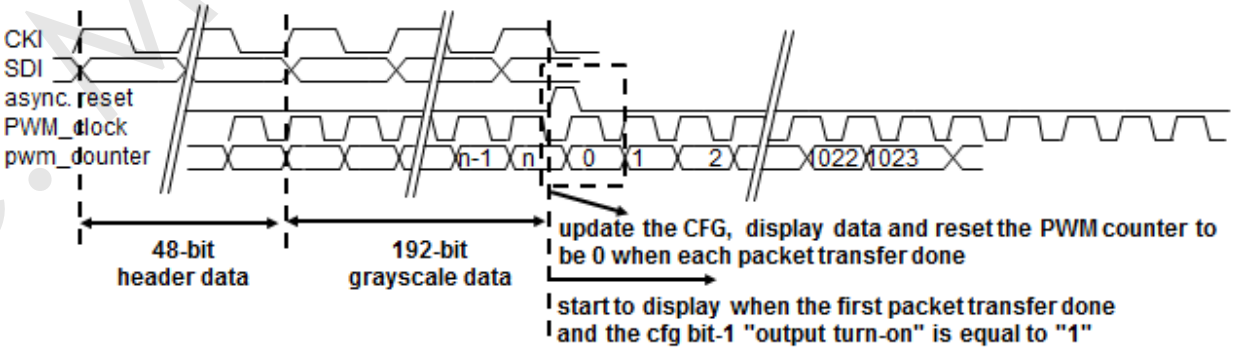
Example of 16-bit Gray Scale with Current Gain



Example of 16-bit Gray Scale without Current Gain



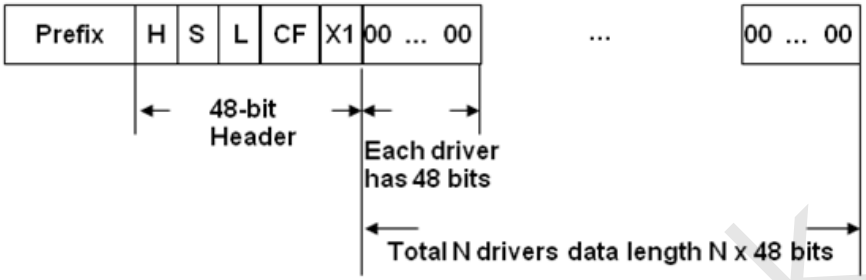




Software Reset

There is a 48-bit header. The header is composed of command data, wait counter data, length data and configuration data. In address data field, always send 14'b00000000000000. Set the number of IC in series to the length data field.

There are 8-bit configuration data in header.
Each driver needs 48-bit zero data.
The software reset command will reset the driver to be initial state.



Prefix
The CKI should be tied-low and stop for more than time-out period (168T x internal OSC) → one CKI pulse (SDI keep) → CKI should be tied-low and stop for more than time-out period (168T x internal OSC)

48-bit header

Bit	Definition	Value	Function
47:40	H[7:0]	8'b11000001	The command of packet
39:26	S[13:0]	14'b00000000000000	Wait counter data. Always send 14'b 00000000000000
25:12	L[13:0]	N -1 N=Number of IC in series	Set the number of IC in series. In unmixed connection mode: L[13:10] don't care, Only the L[9:0] are effective. In mixed connection mode: L[13:12] don't care, Only the L[10:0] are effective.
11:4	CF[7:0]	8'hxx	Don't care.
3:0	X1[3:0]	4'hx	Don't care.

Output Polarity Change (IC to work as a PWM controller)

MBI6033 can be used as a PWM controller in applications that would require large driving currents, such as stage lights, by utilizing the POL pin of the driver IC.

Pin 22 of GP/GTS package
Pin 15 of GFN package

POL pin = High → PWM controller mode

1. The output channel is high active
2. Only operable with none current gain. The command and input data type should be the same as without current gain data.

POL pin = Low (default) → constant current mode

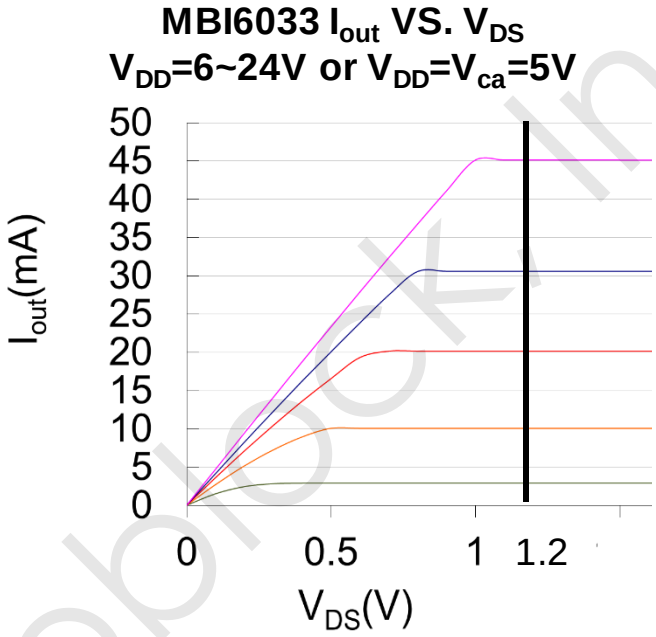
1. The output channel is low active
2. Openable with or without current gain, the command and input data type follows accordingly.

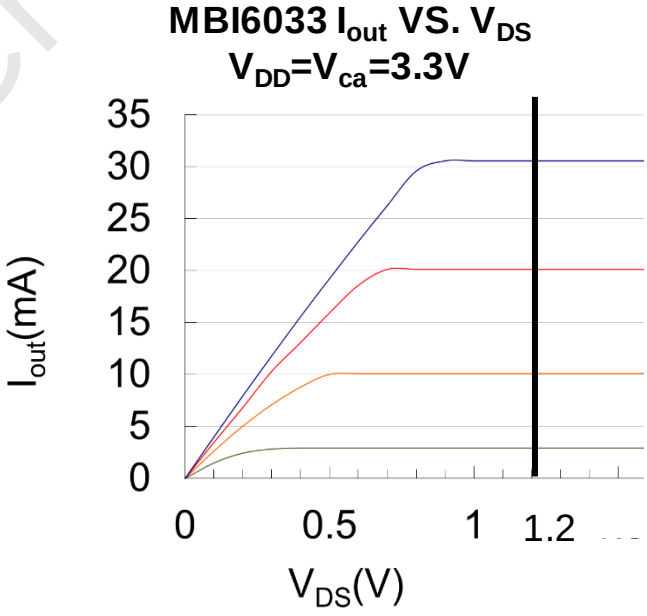
Please refer to the *"MBI6033 Application Note"* for more information on how to setup as a PWM controller.

Constant Current

1) MBI6033 performs excellent current skew: the maximum current variation between channels is less than ±3%, and that between ICs is less than ±6%.

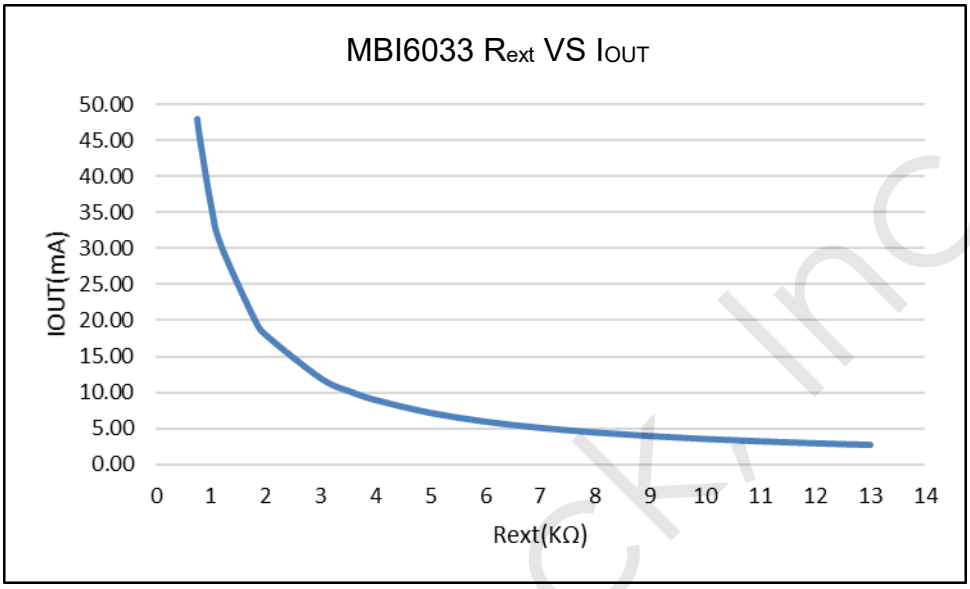
2) In addition, in the saturation region, the output current keeps constant when the output voltage (V_{DS}) is changed. This characteristic guarantees the LED show the same brightness regardless of the variations of LED forward voltages (V_F).





Setting the Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.



The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. When output channels are turned on, V_{REXT} is around 0.6V. The relationship between I_{OUT} and R_{ext} is shown in the following figure.
Also, the output current can be calculated from the equation:

$I_{OUTA0\sim A3} = (V_{REXT} / R_{ext}) \times 60 \times (CG_A / 127)$
$I_{OUTB0\sim B3} = (V_{REXT} / R_{ext}) \times 60 \times (CG_B / 127)$
$I_{OUTC0\sim C3} = (V_{REXT} / R_{ext}) \times 60 \times (CG_C / 127)$

a.) 7-bit Current gain weighting $CG_A/CG_B/CG_C$, default is 127(16'h7F)
b.) The V_{REXT} is around 0.6V.
c.) R_{ext} is 12KΩ (3mA) to 0.8KΩ (45mA)

$CG_A = A6 \times 2^6 + A5 \times 2^5 + A4 \times 2^4 + A3 \times 2^3 + A3 \times 2^3 + A2 \times 2^2 + A1 \times 2^1 + A0 \times 2^0$
$CG_B = B6 \times 2^6 + B5 \times 2^5 + B4 \times 2^4 + B3 \times 2^3 + B3 \times 2^3 + B2 \times 2^2 + B1 \times 2^1 + B0 \times 2^0$
$CG_C = C6 \times 2^6 + C5 \times 2^5 + C4 \times 2^4 + C3 \times 2^3 + C3 \times 2^3 + C2 \times 2^2 + C1 \times 2^1 + C0 \times 2^0$

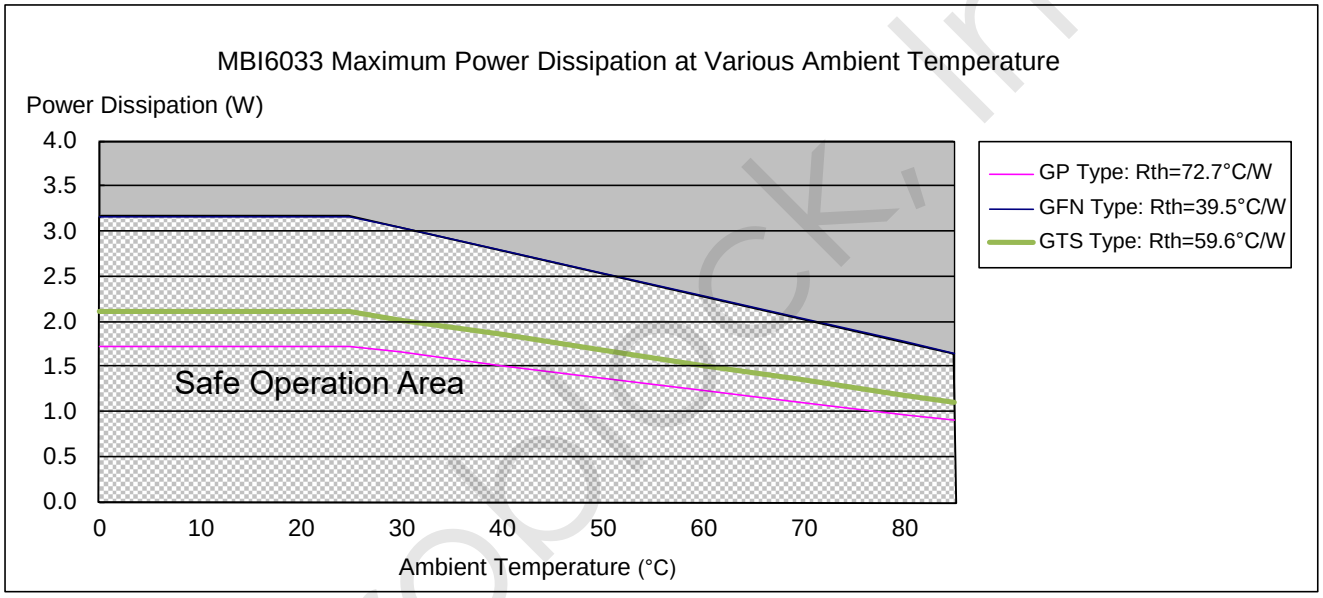
Package Power Dissipation (P_D)

The maximum power dissipation, $P_D(max)=(T_{j,max}–T_a)/R_{th(j-a)}$, decreases as the ambient temperature increases.

The power dissipation (P_D) is calculated by the equation:

$P_D = (V_{DD} \times I_{DD}) + (I_{OUTA} \times V_{DSA}) + (I_{OUTB} \times V_{DSB}) + (I_{OUTC} \times V_{DSC})$

Please refer to the following figure to design within the safe operation area.



Load Supply Voltage (V_{LED})

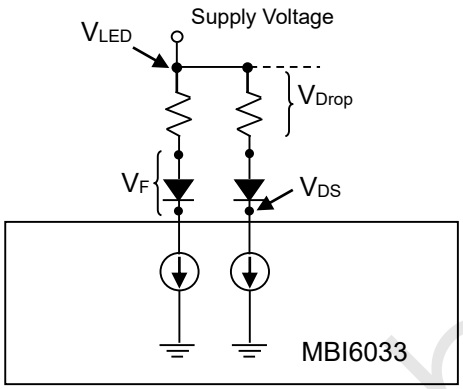
The design of V_{LED} should fulfill two targets:

1. Less power consumption and heat
2. Sufficiently headroom for the LED and driver IC to operate in the constant-current region.

From the figure below, $V_{DS}=V_{LED}–V_F$, which V_{LED} is the supply voltage of LED. $P_{D\ (act)}$ will be greater than $P_{D\ (max)}$, if V_{DS} drops too much voltage on the driver. In this case, it is recommended to use the lowest possible supply voltage or to set an external resistor to reduce the by V_{DROP}.

$V_{DS}=(V_{LED}–V_F)–V_{DROP}$

Please refer to the following figure for the application of the resister.

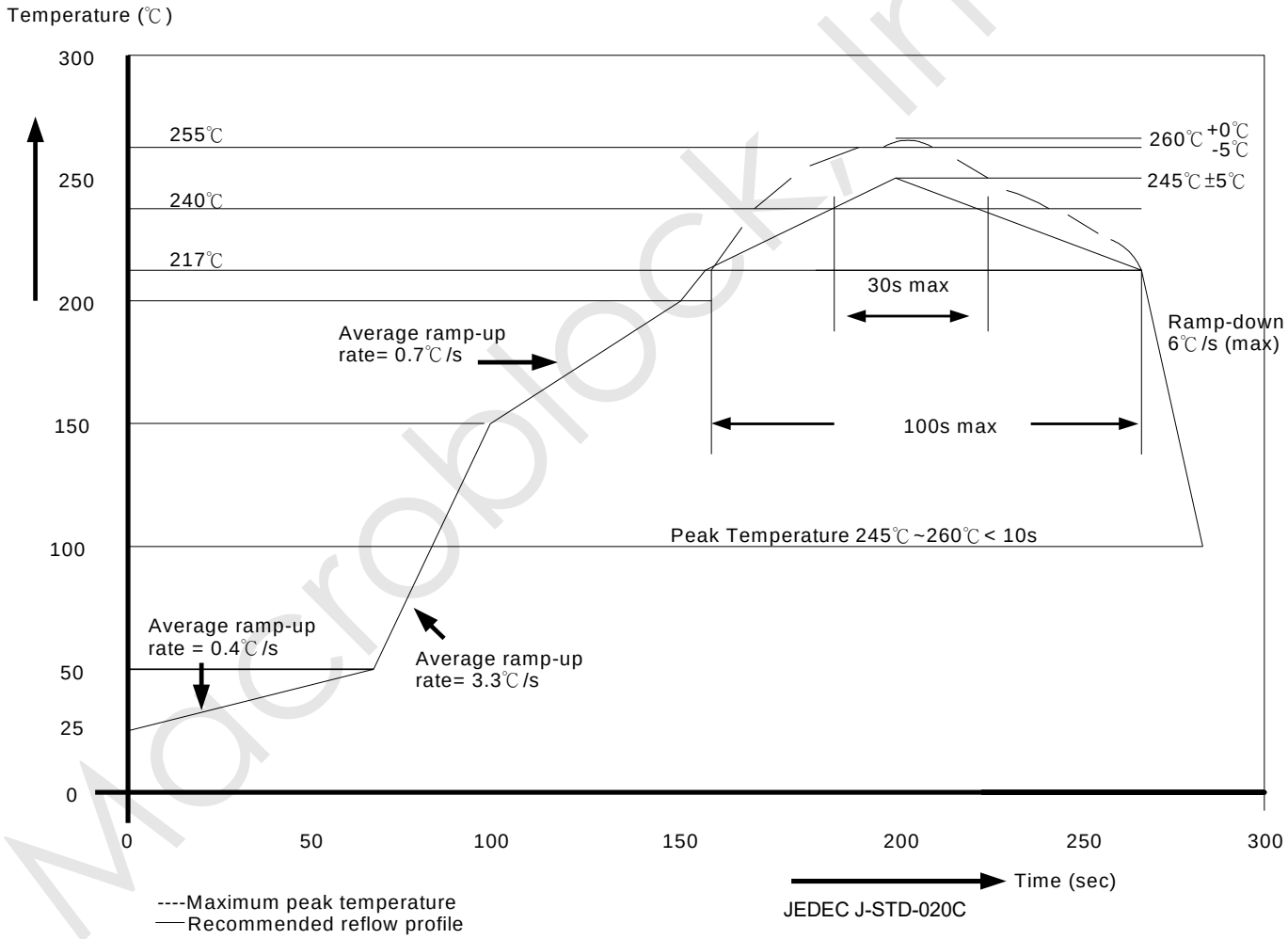


Switching Noise Reduction

The output ports of LED drivers are frequently switching in typical applications. This behavior usually causes switching noise due to the parasitic inductance on PCB. To eliminate switching noise, please refer to “Application Note for 8-bit and 16-bit LED Drivers-Overshoot”.

Soldering Process of "Pb-free & Green" Package Plating*

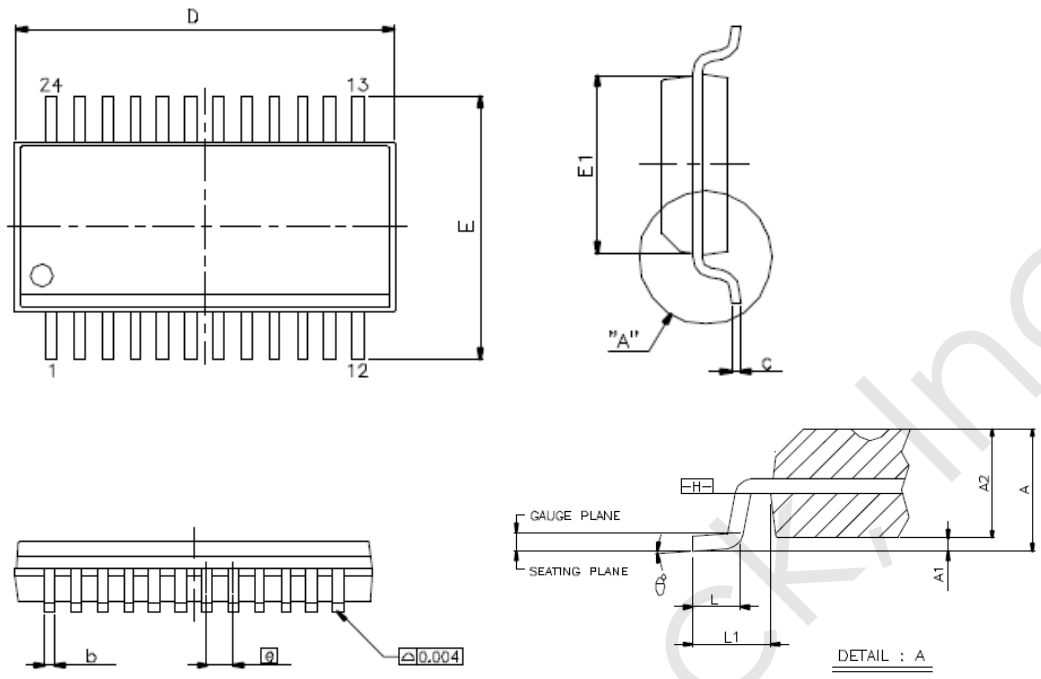
Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to reflow processes which adopt tin/lead (SnPb) solder paste. Please refer to JEDEC J-STD-020C for temperature setting. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.



Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

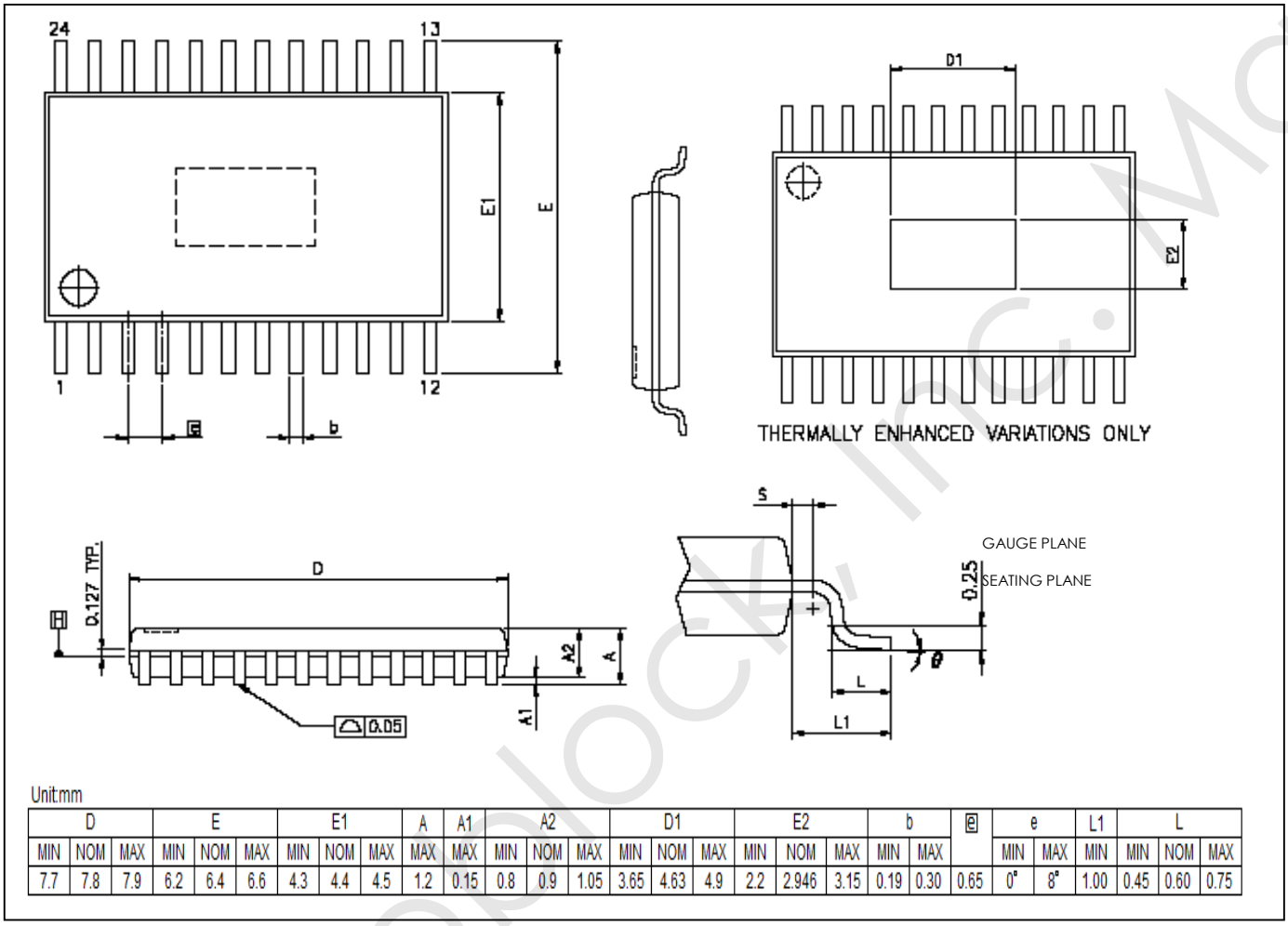
*For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
θ°	0	—	8	0	—	8

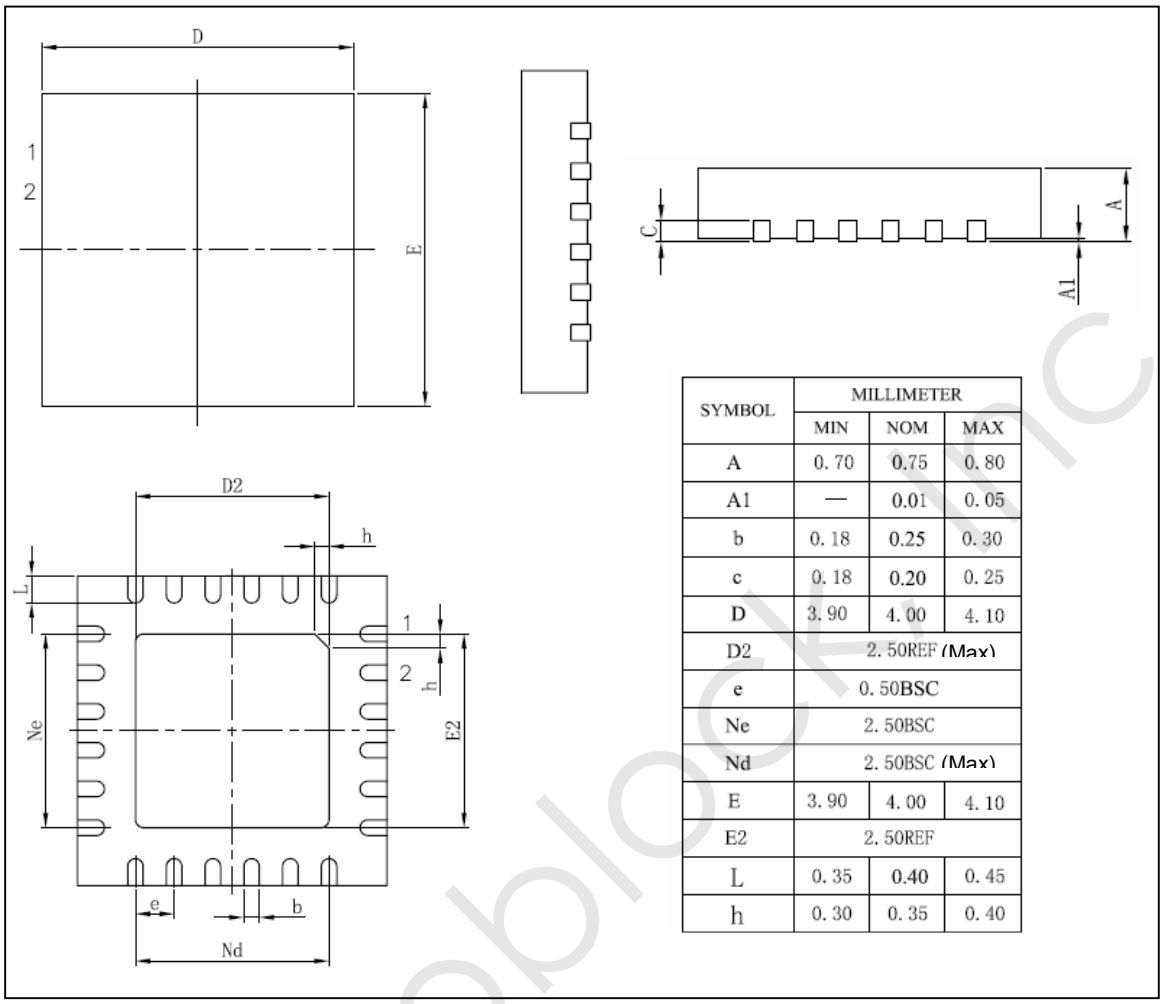
MBI6033GP Outline Drawing



Unit:mm

D			E			E1			A	A1	A2			D1			E2			b		e		L1	L		
MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MAX	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	MAX	e	MIN	MAX	MIN	MIN	NOM	MAX
7.7	7.8	7.9	6.2	6.4	6.6	4.3	4.4	4.5	1.2	0.15	0.8	0.9	1.05	3.65	4.63	4.9	2.2	2.946	3.15	0.19	0.30	0.65	0°	8°	1.00	0.45	0.60	0.75

MBI6033GTS Outline Drawing



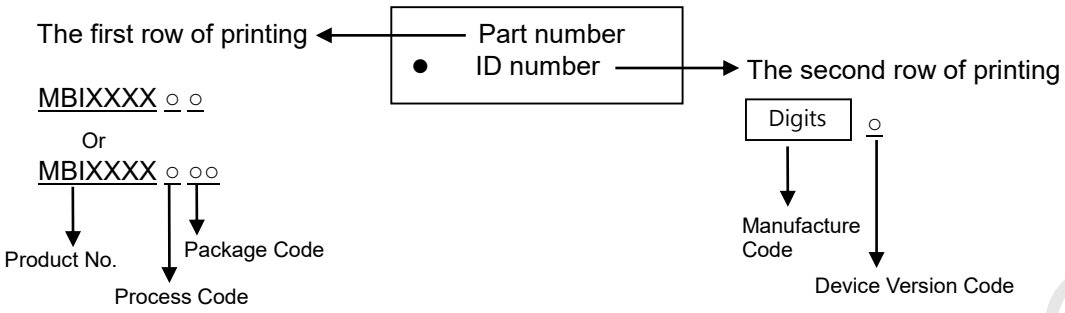
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.01	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	3. 90	4. 00	4. 10
D2	2. 50REF (Max)		
e	0. 50BSC		
Ne	2. 50BSC		
Nd	2. 50BSC (Max)		
E	3. 90	4. 00	4. 10
E2	2. 50REF		
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40

MBI6033GFN Outline Drawing

Note 1: The unit for the outline drawing is mm.

Note 2: Please use the maximum dimensions for the thermal pad layout. To avoid the short circuit risk, the vias or circuit traces shall not pass through the maximum area of thermal pad.

Product Top Mark Information



Product Revision History

Datasheet version	Device version code
V2.00	B
V2.01	B
VA.00	B

Product Ordering Information

Product Ordering Number*	RoHS-Compliant Package Type	Weight (g)
MBI6033GP-B	SSOP24L-150-0.64	0.11
MBI6033GTS-B	TSSOP24-173 -0.65	0.0967
MBI6033GFN-B	QFN24L-4*4-0.5	0.0379

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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